General Description

The low noise differential CiTIA can be used as an Isolator circuit where it has inherent concurrent signal separation/ isolate >120dB. Any signal can be simultaneously transmitted on an antenna or wire, while concurrently receiving any other signal on the same antenna or wire, without restrictions (from the noise floor to signal clipping) of signal shape, bandwidth, amplitude, or frequency, manifesting true full duplex communication. In addition to communication, this has a wide application in sensors which can be integrated into ANY DIGITAL CMOS IC process, not needing analog extensions.

Typical Applications

- Telecommunications
- Low Noise Preamplifiers (LNA)
- Combined Analog and Digital System-on-Chip (SoC)
- Signal Isolator
- Sensing
- Modulation/Demodulation
- Logic Signal Transmission
- Bus Line Receiver
- Accurate and fast Analog Signal Level Transmission
- Fiber Optic Receiver, and many more.

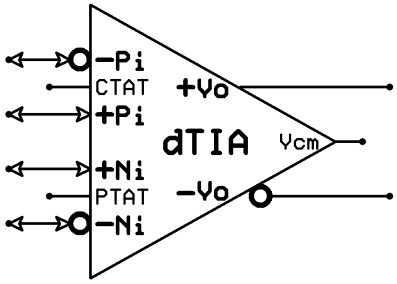

Figure 1. Differential CiTIA Symbol

Features

Works in **any** IC process — no IC process extensions thus enabling portability between IC process including FinFETs
Amplifier harmonic distortion: -160dB (10-Million:1 or 24 bits digital resolution)
9+ decade concurrent signal isolation: >120dB (signal separation ratio of 250-Million:1 or 28 bits digital resolution)
Wide bandwidth: linear output from DC to ~50GHz and beyond for nanoscale IC processes
Low power consumption: About 140µW at 1.8V or 2µW at 1V [V_{DD}]
Supply voltage: 2V down to 500mV or from IC Process Limit (extends down to 10mV V_{DD} at slower speeds)
Self-biasing with adjustable trans-impedance gain and offset control options
A_V (Open Loop trans-impedance Gain): 35dB (over a 0.8V to 1.8V V_{DD}) and can be combined with other CiFET amplifiers for any gain
Full-Differential input and output available with output swings approaching rail-to-rail
Zero-crossover Distortion, floating open circuit inputs allowed, and iPort analog inputs can be wire-ORed
Ability to match a low impedance antenna or a moderate input resistance (35KΩ) for instrumentation charge sensing
Dual bi-directional additive complementary I/O current ports useful as an ultra-linear modulator
Adjustable low input impedance to match signal sources and transmission lines
Common-mode virtual-ground and PTAT/CTAT reference voltage outputs available
Voltage-forced single-ended or differential outputs with a moderately low active output impedance
No restrictions on relative bi-directional input current signal magnitude from noise floor to saturation
No output crossover distortion including zero open circuit inputs allowed
No restrictions on waveform shape or frequency
No restrictions on low transmission line or antenna signal source impedance

NOTE: *Results are based on a 180nm EKV simulation model. As process shrinks, performance scales with logic speed*.

Electrical characteristics

** Low R_{out} obtained by paralleling multiple output CiFET stages*
*** R_{out} over power supply voltage down to 0.5V*

Table 1. T_A=25 °C, 180nm Digital Technology Example (improves proportional to process shrink)

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
Input Voltage Range						
I_{CMR}	Input Common-Mode range		--	+10	±100	µV
Input Bias Current and Impedance						
R_{in}	Input Resistance	Low R_{in} configuration	25	100	600	Ω
		Instrumentation cfg.	1K	25K	100K	
Trans-Impedance Gain						
A_{OL}	Open-Loop Trans-impedance Gain	V_{DD} = 800mV	--	38	--	dB
		V_{DD} = 1.0 V	--	37	--	dB
		V_{DD} = 1.2V	--	35	--	dB
		V_{DD} = 1.8 V	--	31	--	dB
Output						
V_{OUT}	Maximum Voltage Swing	V_{DD} = 1.8 V	V_{SS}	--	V_{DD}	mV
V_{OSR}	Linear Output Swing Range	V_{DD} = 1.8 V	V_{SS}	--	V_{DD}	mV
	Maximum Differential Output Swing	V_{DD} = 1.8 V	V_{SS}	~2xV_{DD}	--	V
R_{OUT}	Output Resistance*	V_{DD} = 1.8 V	1K	5K	10K**	Ω
R_{LOAD}	Resistive Load*	V_{DD} = 1.8 V	10K	50K	∞	Ω
C_{LOAD}	Capacitive Load Drive	V_{DD} = 1.8 V	0	--	200	fF
	Linearity	V_{DD} = 1.8 V	-120	-140	-160	dB
	Crossover Distortion	V_{DD} = 1.8 V		none		dB
Power Supply						
V_{DD}	Supply Voltage		0.5	1	2	V
I_Q	Quiescent Supply Current	V_{DD} = 1.0 V	--	3µ	--	A
		V_{DD} = 1.8 V	--	140µ	--	A
P_Q	Power Consumption	V_{DD} = 1.0 V	--	1µ	--	Watts
		V_{DD} = 1.8 V	--	125µ	--	Watts
Temperature Range						
T_A	Operating Range		-55	25	125	°C
	Extended Temperature Range		-150	--	250	°C
Frequency Response						
BW	Bandwidth	R_{LOAD} = 50Ω	50	--	>100	GHz
PM	Phase Margin	V_{DD} = 1.8 V	--	61	--	°
t_{OR}	Overload Recovery Time	V_{DD} = 1.8 V	--	10	--	pS
FBW	Full-power Bandwidth		--	1	>100	GHz
Noise						
e_n	Input Voltage Noise (Voltage Amplifier)	10 kHz	--	-120	--	dB {nV/√Hz}
		10 kHz	--	2	--	nVPP
V_n	Input Voltage Noise Density	10 MHz	--	-150	--	dB {nV/√Hz}
I_n	Input Current Noise Density	10 MHz	--	-180	--	dB {nA/√Hz}
		1 GHz	--	-200	--	dB {nA/√Hz}

50Ω example

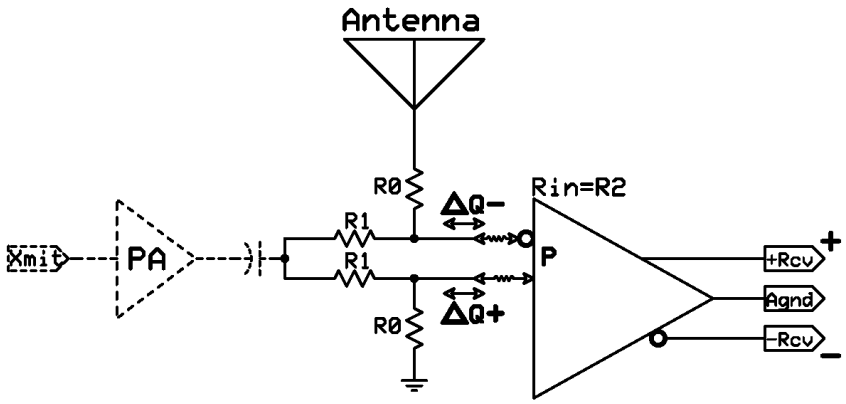

Figure 2. Full-differential CiTIA — Isolator application example (signal input is charge transfer into a real termination resistance)

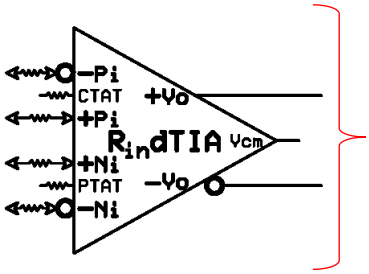

Figure 3. Complete Differential CiTIA symbol

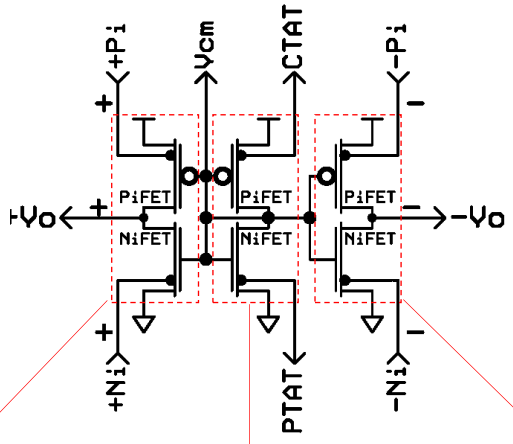

Figure 4. Differential CiTIA schematic

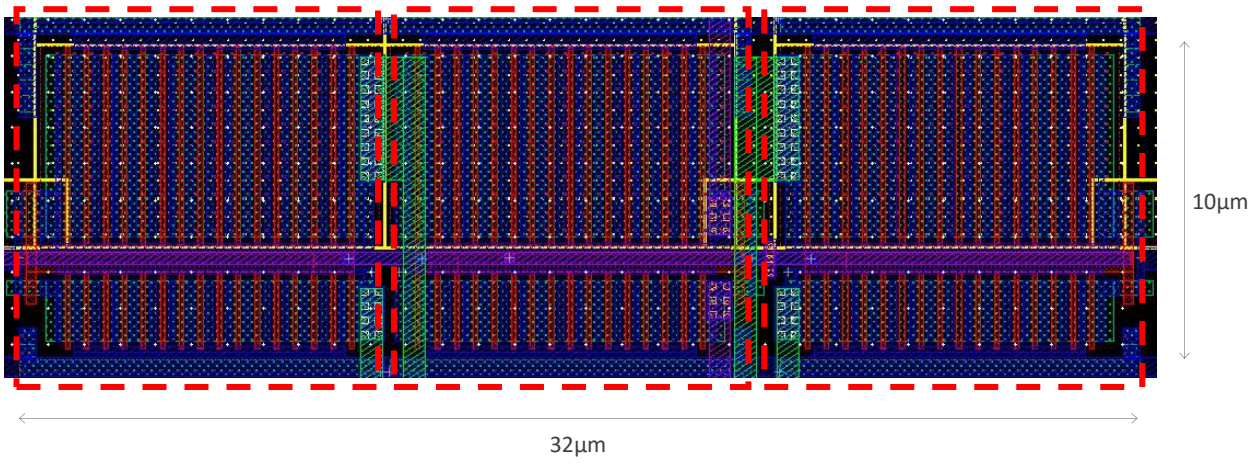

Figure 5. Differential 50Ω CiTIA, Trans-impedance Gain = 80dB from an iFET ratio of 128 (130nm example)

Differential CiTIA Isolator (100Ω antenna) — dynamic signal separation range

Isolating 1 decade of signal amplitude difference

Isolating **10 decades** of signal amplitude difference

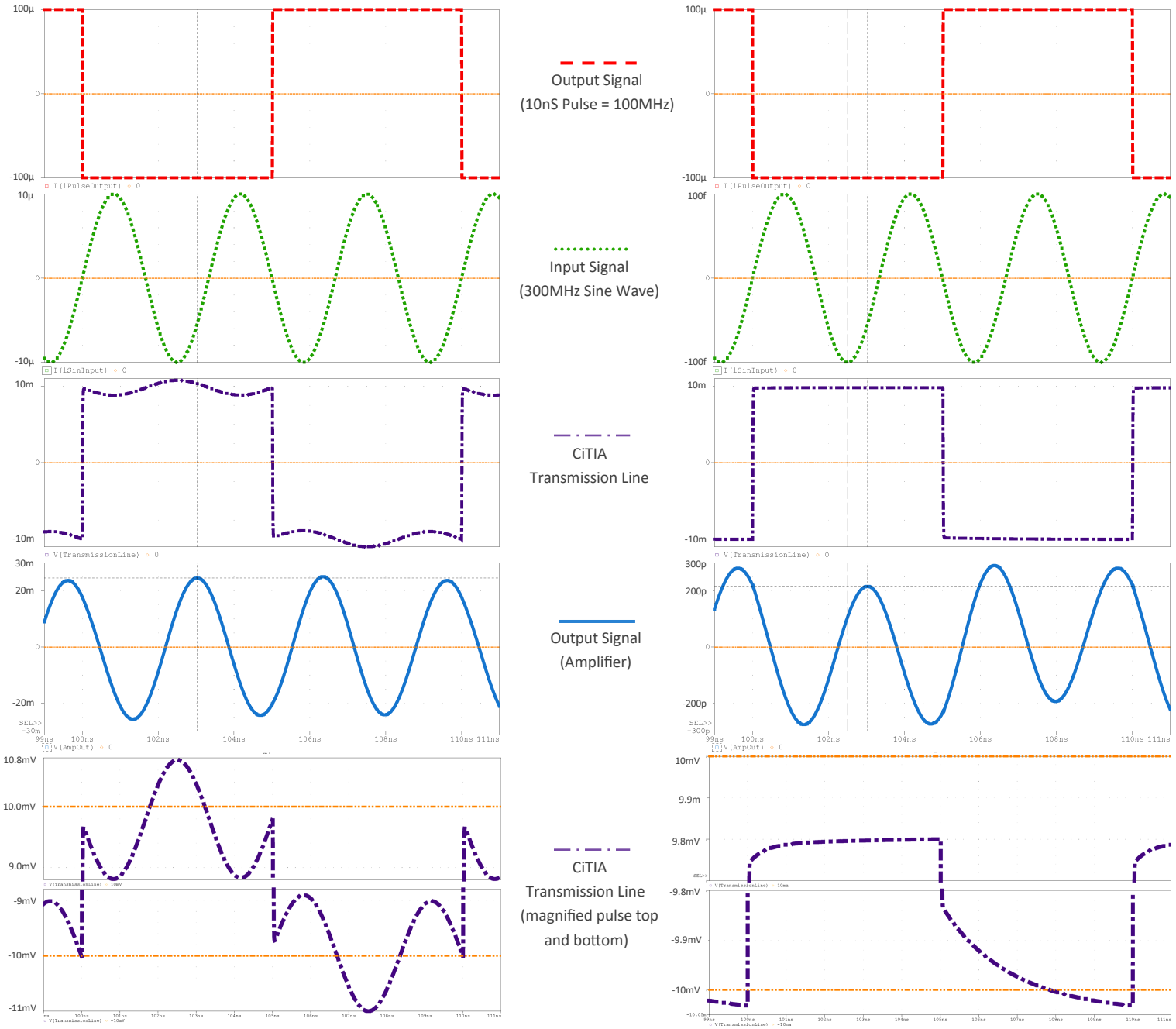

Figure 6. Differential CiTIA Isolator with a high **1mv** (=10µa) 300MHz sine wave downlink signal separated from a ***1 decade higher concurrent* 10mv** (=100µa) 10ns [100MHz] pulse uplink

Figure 7. Differential CiTIA Isolator with a microscopic **10pv** (=100fa) 300MHz sine wave downlink signal separated from a ***10 decade higher concurrent* 10mv** (=100µa) 10ns [100MHz] pulse uplink

The Antenna of the Differential CiTIA Isolator of Figure 2 is driven by a 100uA pulse uplink signal by the Power Amp (PA) while concurrently receiving a smaller downlink sinewave signal on the same antenna. The composite antenna signal voltage is the middle waveform, with magnified top and bottom regions as the lower waveforms. The solid blue sinewave = amplified downlink received.

CiTIA— Full-Duplex stealth communications

The transmitted signal can be turned around and retransmitted, leaving no apparent signal on the antenna or transmission line.

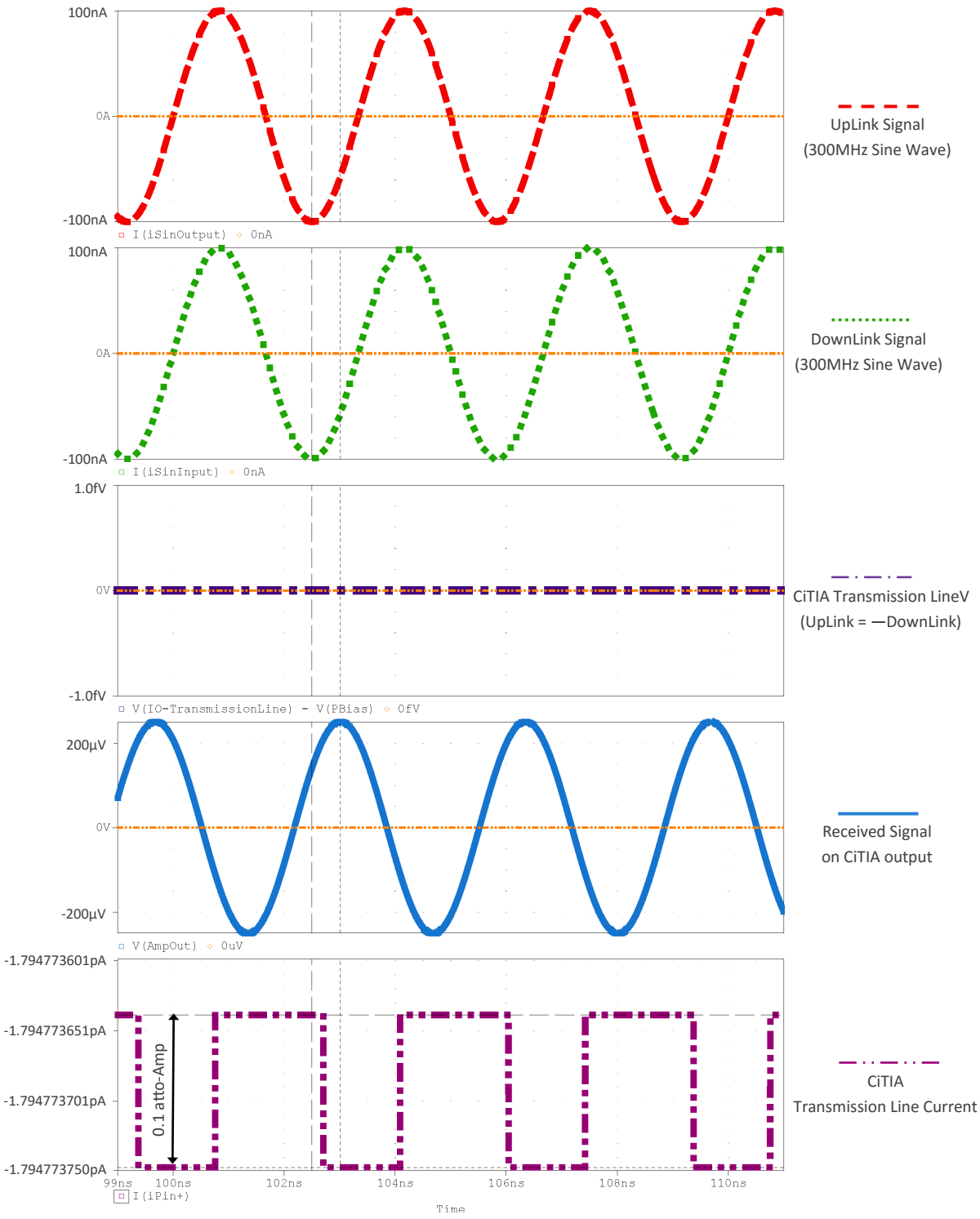

Figure 8. Differential CiTIA Extracting and Masking a 300MHz 100na Sine Wave Signal on a 100Ω Line.

Differential CiTIA Isolator (100Ω antenna) — operates with **ANY** Vdd

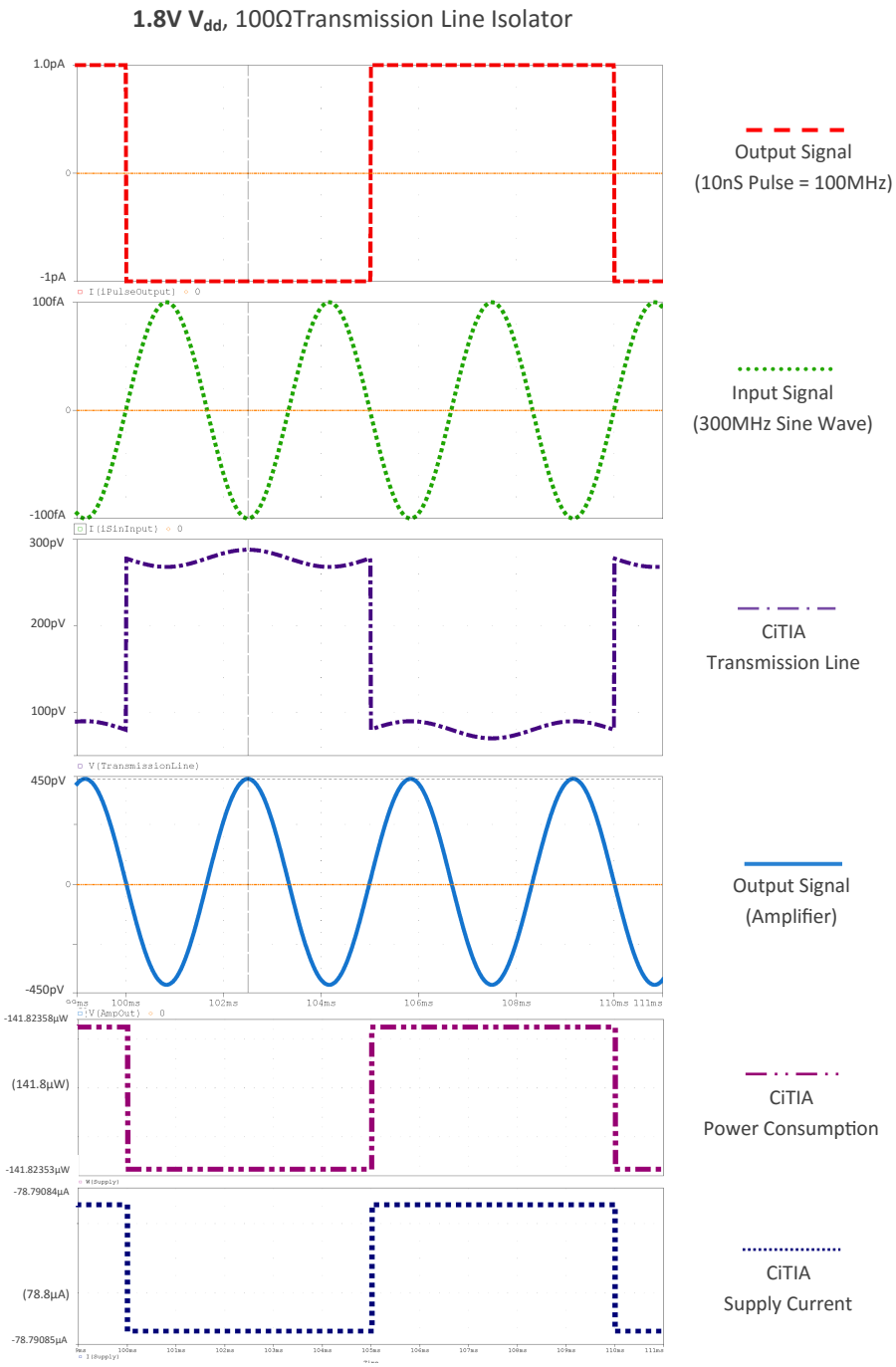

Figure 9. Differential CiTIA Isolator with a ± 100pv (± 1pa) 100Hz (10ms) square-wave output signal, separated form a ***concurrent*** ± 10pv (± 100fa) 300Hz sine wave input signal, on a 100Ω transmission line, running off a V_{dd} = 1.8V.

The supply current and power dissipation are the lower pair of waveforms — note that the CiTIA is not limited by threshold voltage. Without a power supply, the CiTIA powers off its input signals and remains operational at the input frequencies, reminiscent of forgetting to turn on the CMOS logic power supply that we all have done at one time or another.

CiTIA harmonic distortion

100µV (1µA) at 10KHz sine wave into the CiFET TIA configured as a 100Ω Rin Low Noise Amplifier with a trans-impedance gain of 43

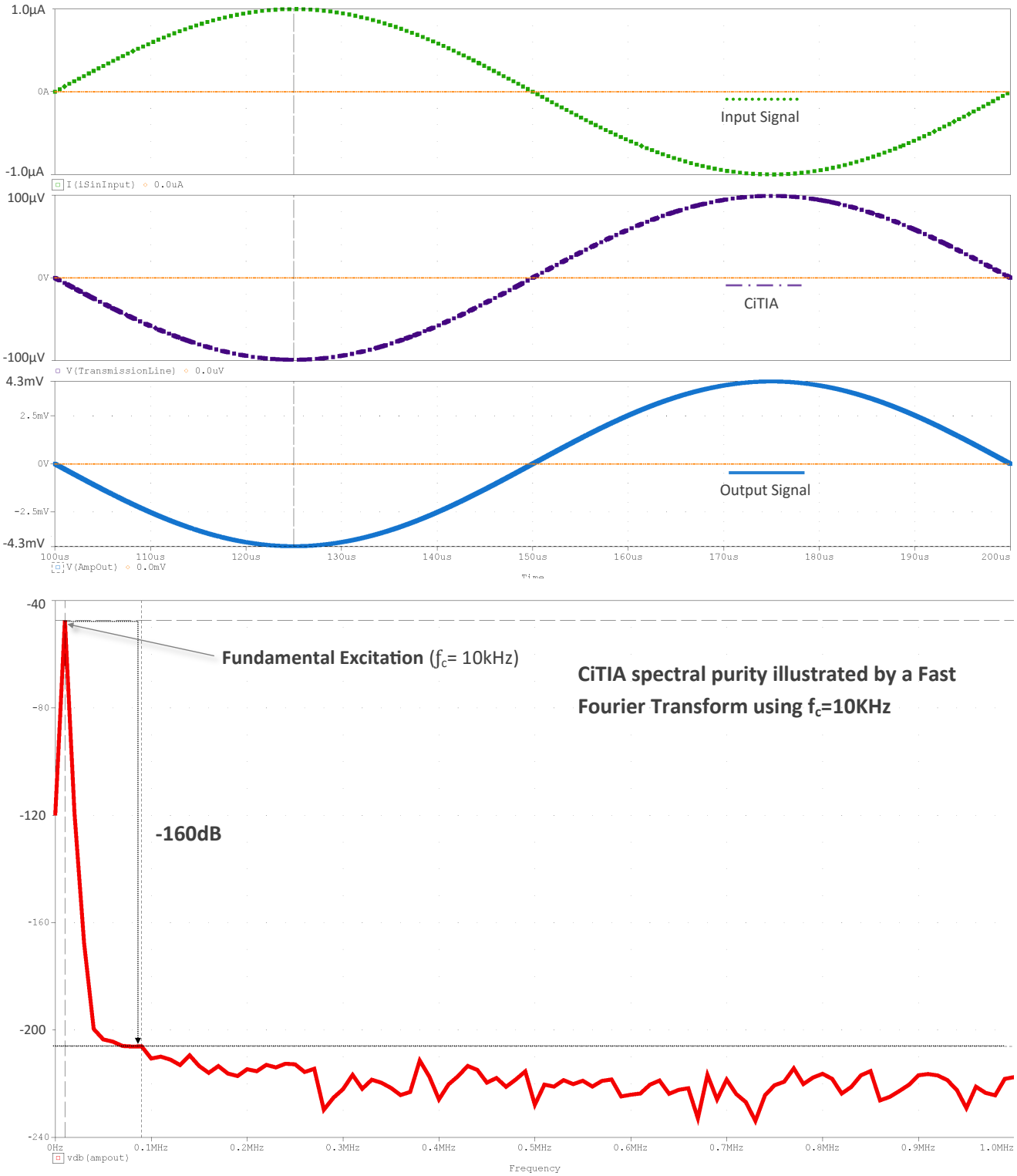

Figure **10.** FFT output frequency spectrum of a 100Ω differential CiTIA running a **1µA** - 10KHz sine wave input

CiTIA harmonic distortion when overdriven at 0.1V (1mA) input at 10KHz)

Input overdriven with 100mV (1mA) at 10KHz sine wave into the CiFET TIA configured as a 100Ω Rin Low Noise Amplifier

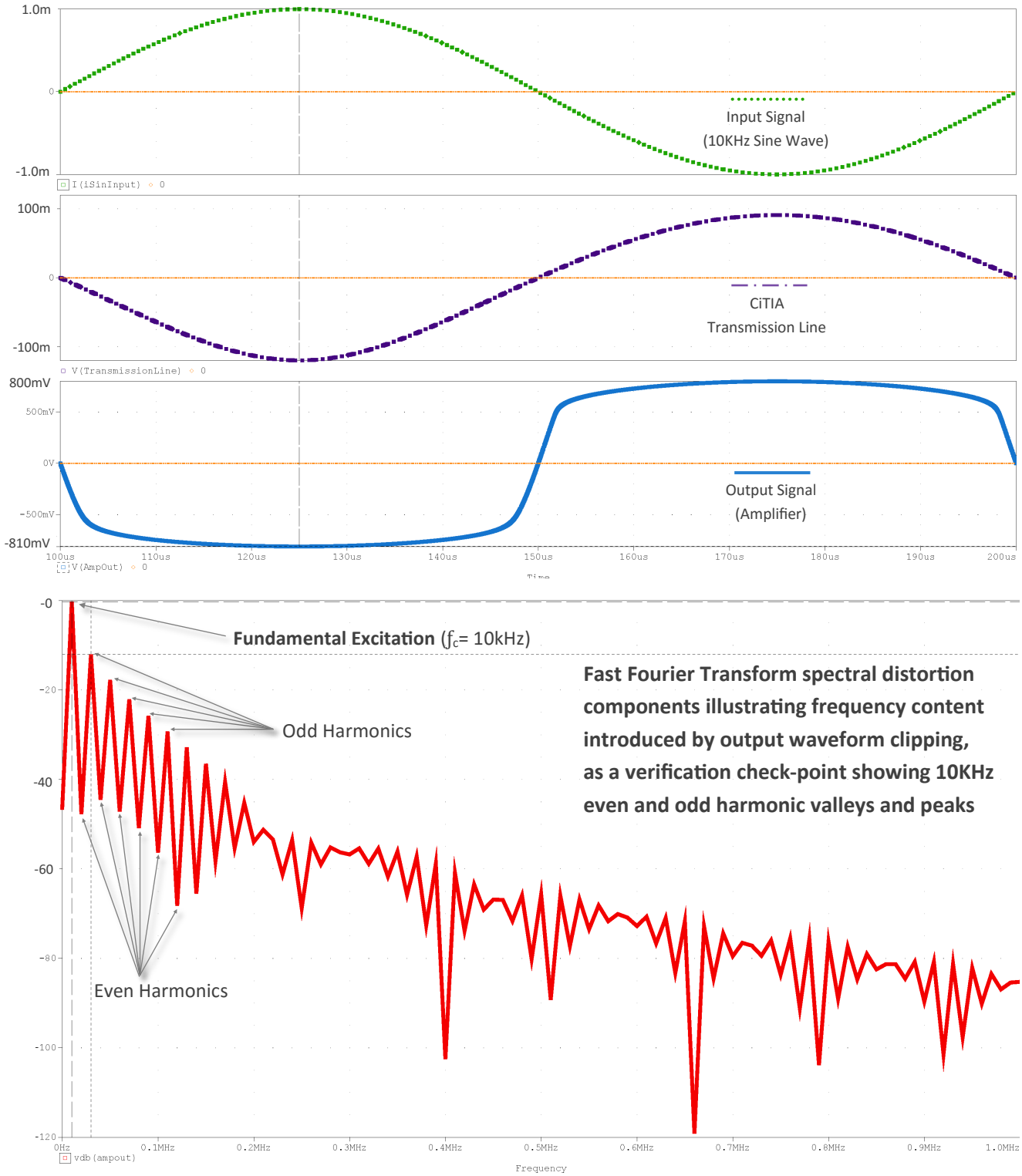

Figure 11. Differential CiTIA 100Ω Isolator driven with **100mV (1mA)** 10KHz spectrally-pure sine wave input

Circuit Seed trans-impedance r_m approach

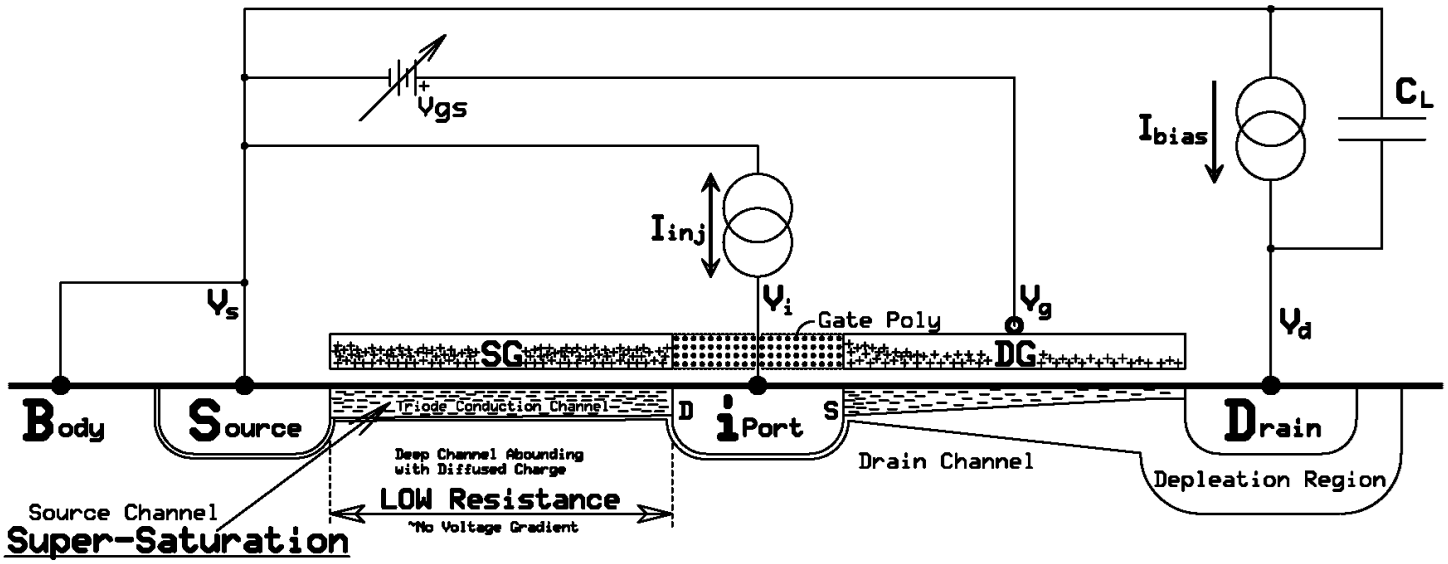

Figure 12. Channel charge distribution in the iFET device during biased operation

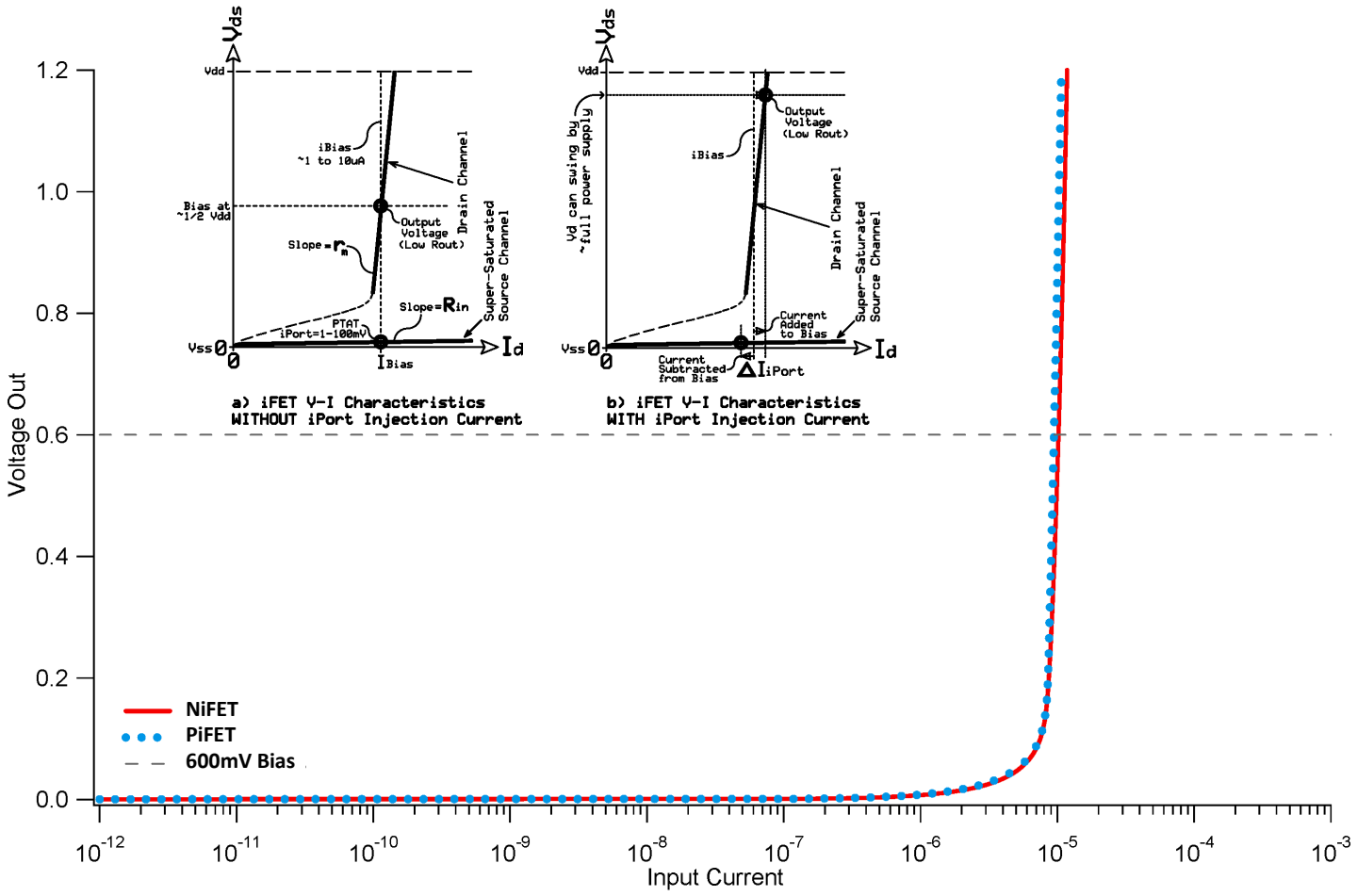

Figure 13. Combined V-I characteristics of a characteristic iFET device with and without input iPort injection current — inserted in the overlaid NiPort and -PiPort injection current to output voltage plot to illustrate the steep transfer function

CiFET detail

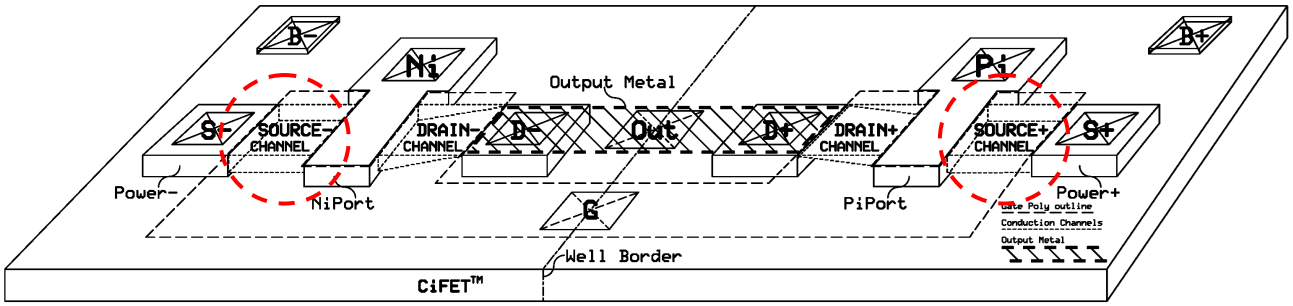

Figure 14. CiFET 3-D Perspective view

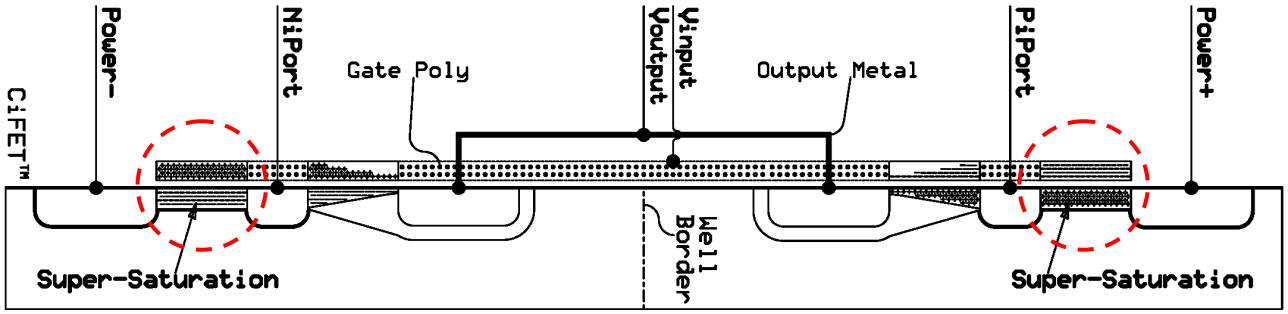

Figure 15. CiFET cross sectional view including biased channel charge concentration

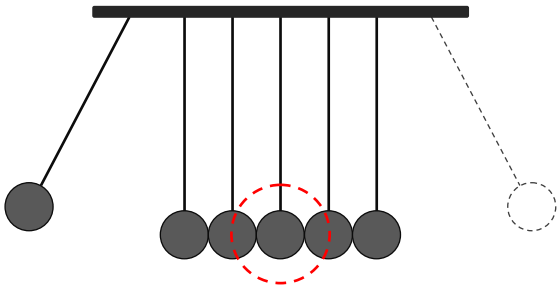

Figure 16. Newton's cradle of collision as an analogy of the super-saturated channel conduction

Charge transmission, or current, is an extremely high-speed mechanism which results from carriers not needing to transit their channel, but instead pass their energy from one carrier to an adjacent carrier similar to Newton's Cradle. Energy transferred through the balls resembles rapid charge movement, illustrating the much higher charge velocity through a dense concentration of charge as being nimble compared to individual charge passing through its channel. Notice that the full signal source energy is transferred into the channel where it is absorbed to instantaneously produce an output signal on the other end.

The first or left-most ball represents the charge entering the super-saturated source channel, which is represented by the chain of balls in contact with one another. The speed of energy being transmitted into the chain is slow in comparison to rapid energy transmission through the chain, where the balls do not move significantly, progressing to the end where the end ball continues to carry the input energy out of the chain of balls. This represents the highly saturated drain channel (which could coincidently go up-hill a bit reflecting an increase in voltage). The energy comes out of the drain channel at an exponential trans-impedance gain (similar to weak-inversion) depending on the drain channel length (representing r_m, the iFET's trans-resistance gain in Ω). Although the r_m is high, the output impedance is low due to the common gate channel configuration and not the anticipated resistance value of r_m.

CiFET sized for a general-purpose signal sensor input stage

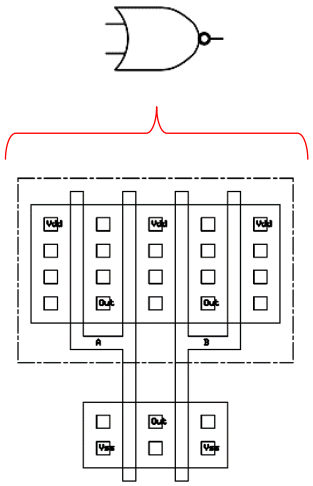

Figure 17. Conventional NOR-2 logic cell layout plan comparison

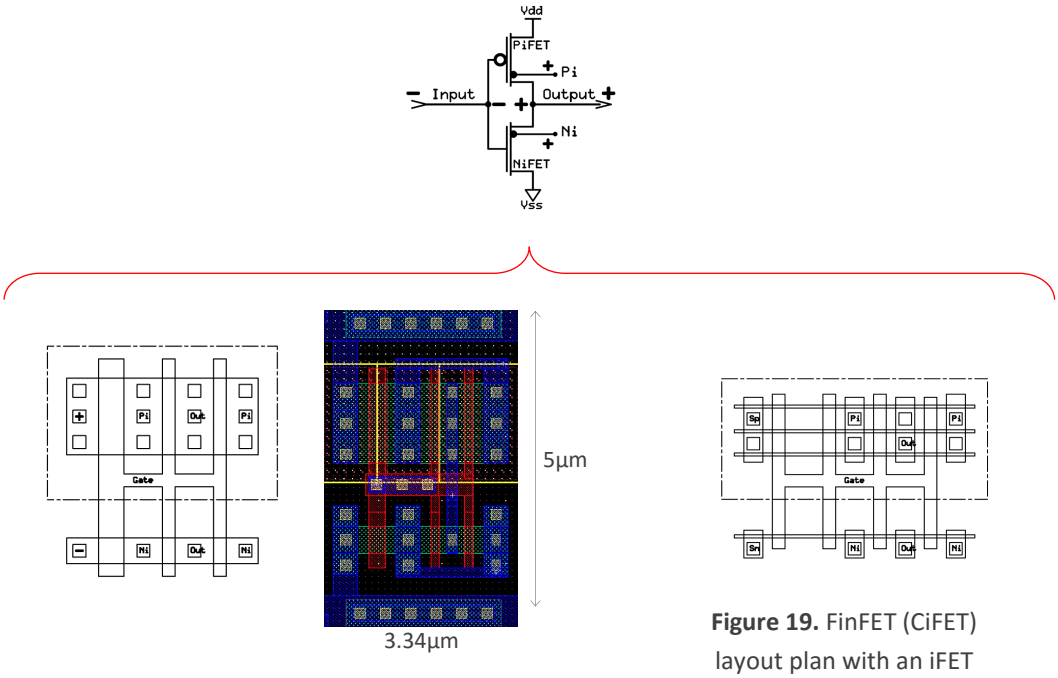

Figure 18. Seminal CiFET layout using the high-trans-impedance gain instrumentation iFET Ratio of 0.25 (IBM/Global-Foundries 130nm)

Figure 19. FinFET (CiFET) layout plan with an iFET Ratio of 0.25

Super-Sensor

The application of a high-r_m CiFET as a high-gain trans-impedance amplifier is branded as the "Super Sensor" distinguishing it for its superior signal capturing significance. This is a fundamental CiTIA application as a general-purpose sensor interface to extract a minute redistribution of electronic charge or the subsequent impedance change within a signal source to be measured electronically. In general, many sensors measure bias current changes controlled by resistance variations, while some measure neurological charge redistribution in an organic system. Neuromorphic circuits model these.

Present analog circuit designs generally accomplish sensing functionality by means of measuring minute voltage changes via a high input impedance voltage amplifier. Thus, sensor interfaces employ a high input impedance voltage controlled input stage to retain the raw signal voltage waveform of the sensor. It is respectable to be able to view the raw sensor voltage, but maximum signal source energy is not transferred into the sensor amplifier, exposing the measured signal to capacitively coupled interference signals and ground noise.

CircuitSeed proposes that analog signal sensing can benefit by employing a trans-impedance amplifier to measure charge (or charge flow) to and from a sensor element. A CiTIA input absorbs charge into its super-saturated CiFET source channel to maximize signal source energy usage efficiency, while converting the measurement to a low impedance voltage output to drive additional signal processing circuitry.

Bipolar and CMOS Op Amps initially convert their input voltage to current and subsequently to voltage, while trans-impedance amplifiers convert their small input current directly to a low impedance voltage. Signal sources typically have a high output impedance making them good signal sources. Because we normally do not like to see a signal voltage source loaded, the soured energy is not normally used, but loading the signal source transfers energy directly into an analog voltage output signal by the amplifier's sensor input.

In voltage amplifiers, the output current is subsequently turned back into a voltage by running this current into a high-impedance load. The CiTIA does this directly. When small analog signal sources are observed with a high impedance voltage amplifier, the sensor output signal is summed with numerous capacitively coupled interferer noise sources to the extent that the sensed output signal may be dependent on where you are standing in the room. High impedance sensing preserves the signal source voltage but encompasses surrounding interference signals. Signal power transfer into the CiTIA can be maximized, when necessary, by matching the iPort input resistance to the signal source resistance by means of selecting the iFET ratio. This R_{in} vs iFET ratio is exemplified in figure 30 plot along with the r_m trans-resistance gain factor.

These CiTIA circuits are fully integrated into any IC process, including processes without any analog IC process extensions, enabling migration into nanoscale processes nodes. Full levels of integration not only have cost savings, but incorporate a system enhancement advantage provided by on chip processing and communication including RF.

Super Sensors in single-ended & differential configurations including self-bias

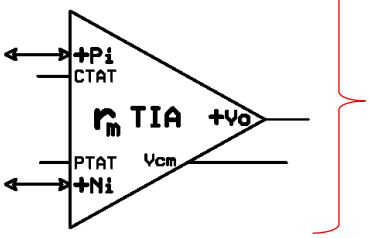

Figure 20. Single-ended high trans-impedance gain CiTIA Super-Sensor symbol

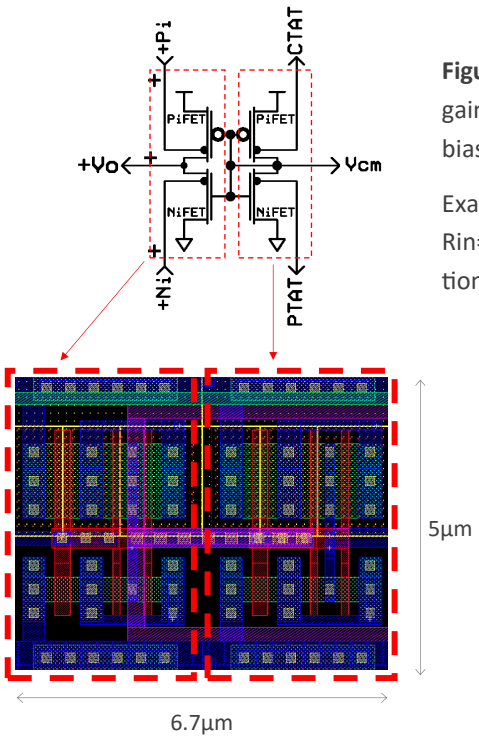

Figure 21. Elementary high trans-impedance gain CiTIA Super-Sensor schematic w/ self-biasing

Example r_m = 1.4 MΩ gain factor yielding Rin=25 KΩ with 200 mV PTAT/CTAT termination from an iFET ratio of 0.25.

Figure 22. Physical layout of a self-biased high gain trans-impedance instrumentation amplifier (r_m = 1.4 Million) CiTIA from an iFET ratio of 1/4

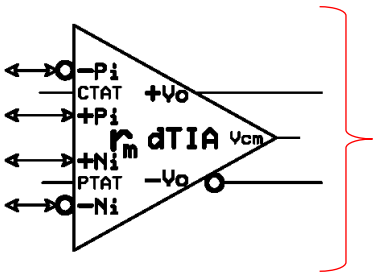

Figure 23. Differential high trans-impedance gain dCiTIA Super-Sensor symbol

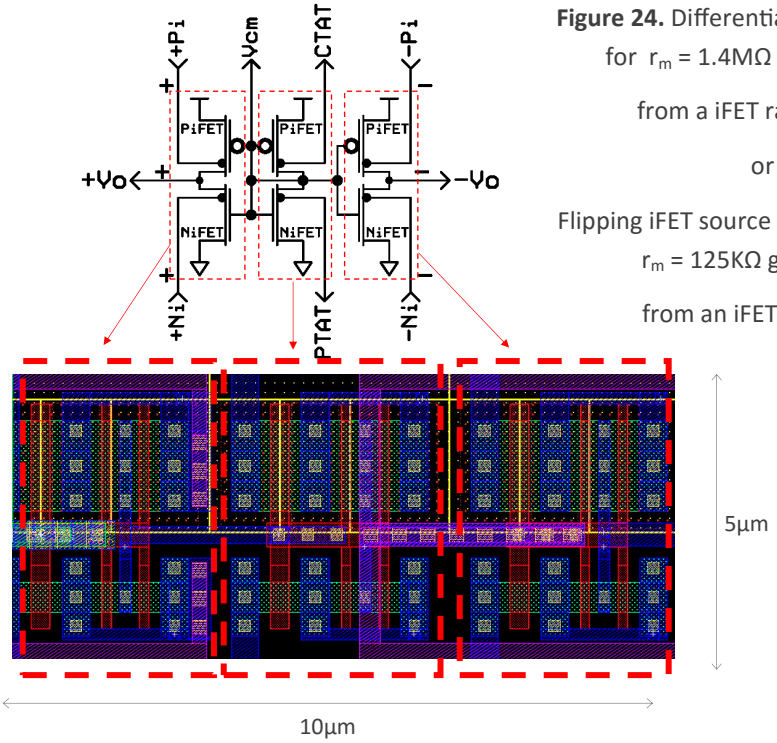

Figure 24. Differential CiTIA schematic for r_m = 1.4MΩ TI gain factor

from a iFET ratio of 1/4

or

Flipping iFET source and drain yields a r_m = 125KΩ gain factor

from an iFET ratio of 4

Figure 25. Differential CiAmp layout with a 1.4MΩ Trans-Impedance Gain from a 1/4 iFET ratio

CiFET linearity over extreme dynamic range

1) Instrumentation iFET ratio = 1/4 forms r_m = 1.4MΩ gain factor with Rin = 25KΩ and PTAT/CTAT termination of 200mV from rails,
or
2) with a flipped iFETs: an iFET ratio = 4 r_m = 125KΩ gain factor is formed with Rin 1.5KΩ and PTAT/CTAT termination at 33mV from rails — plotted in Figure 35, 36, and 37.

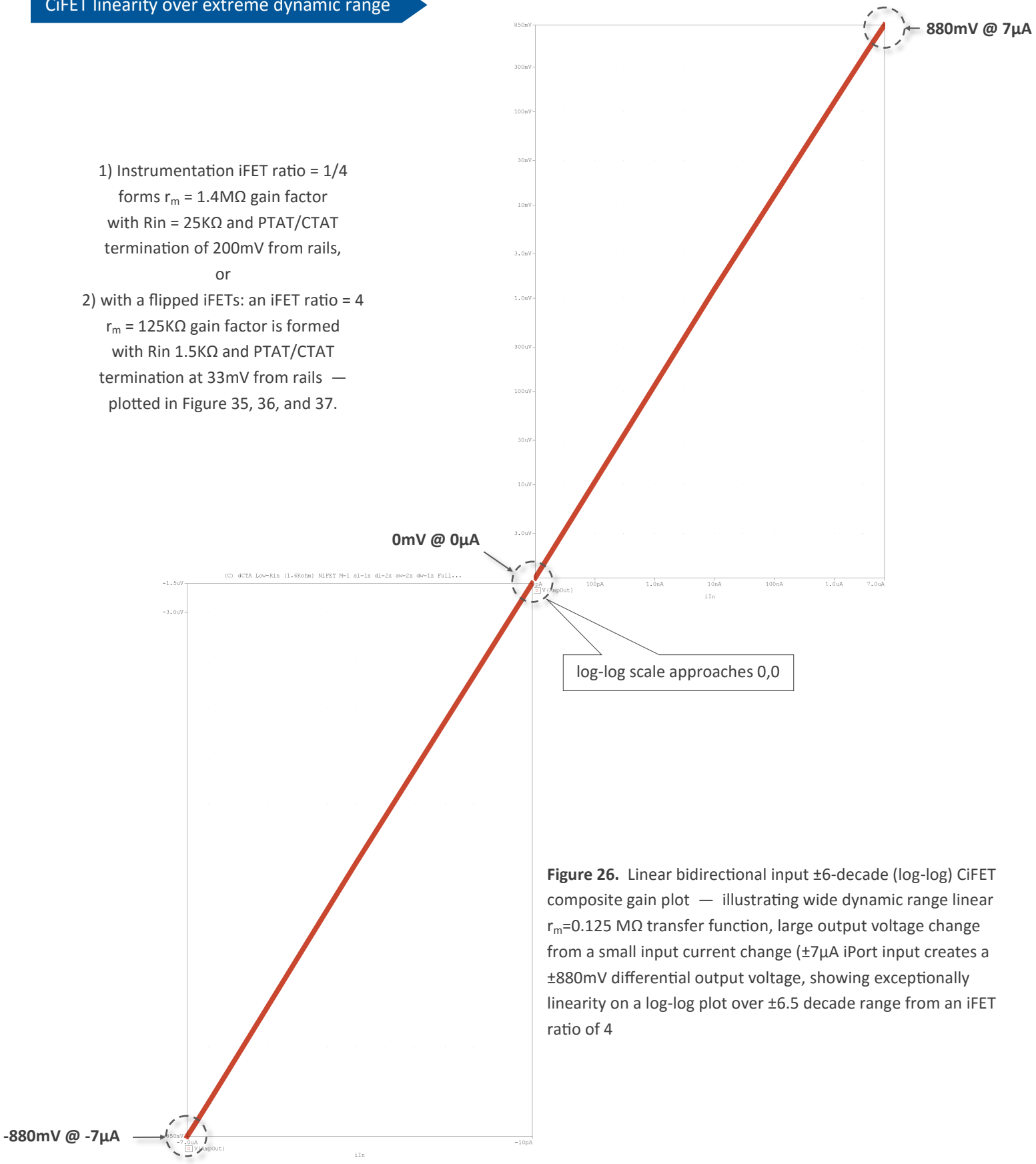

Figure 26. Linear bidirectional input ±6-decade (log-log) CiFET composite gain plot — illustrating wide dynamic range linear r_m=0.125 MΩ transfer function, large output voltage change from a small input current change (±7µA iPort input creates a ±880mV differential output voltage, showing exceptionally linearity on a log-log plot over ±6.5 decade range from an iFET ratio of 4

Rail-to-Rail output voltage linear and saturation regions

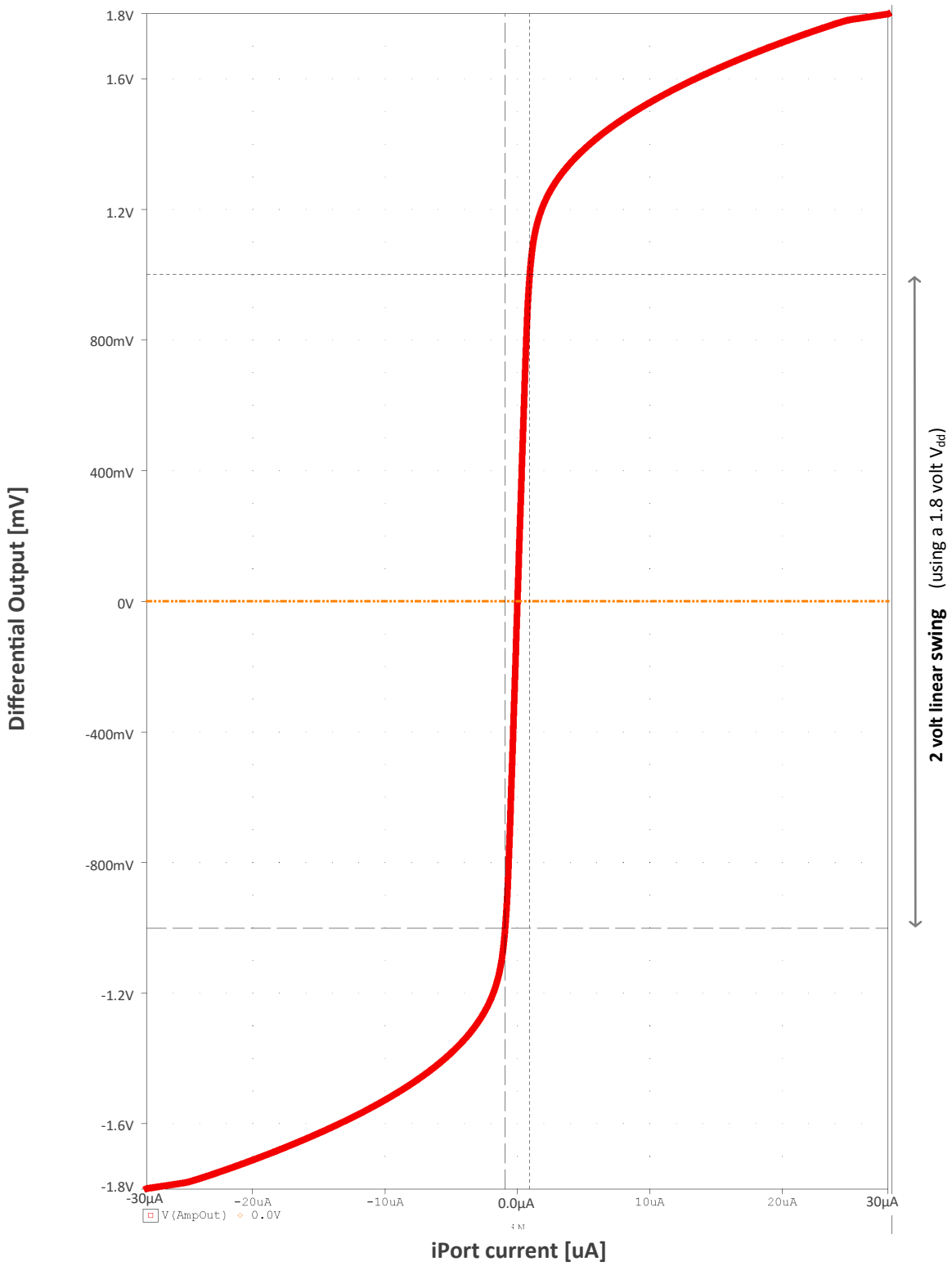

Figure 27. Saturation plot of Rail-to-Rail dynamic output voltage range having a linear region wider than Vdd for a full-differential trans-impedance instrumentation amplifier implemented with a high-gain iFET Ratio of 0.25, yielding rm = 1.4MΩ. All 4 iPort inputs active, showing rm saturation as power rails are approached.

Differential CiTIA iPort modulation

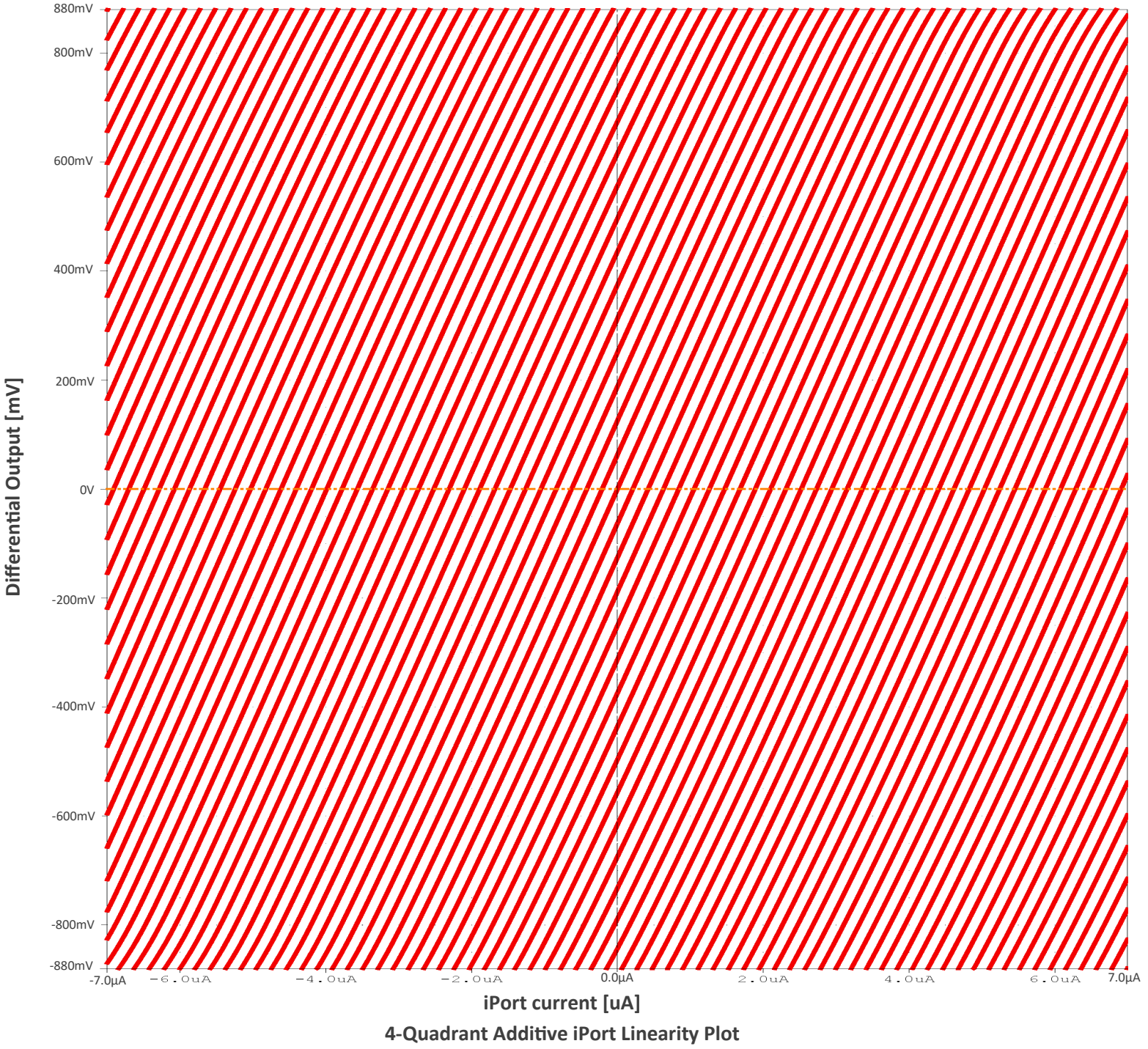

Figure 28. Differential CiTIA as an instrumentation PiPort + NiPort signal adder — illustrates ultra-precise 4-quadrant linear relationship between iPort inputs through sweeping one iPort while the other iPort is stepped for each successive sweep over the entire linear ± dynamic operating range. Since the differential CiTIA has 4 iPort inputs, 4 input signals can be modulated onto the same output. Another summing method is to wire-or multiple current inputs into any of the iPorts. All 4 iPort inputs are active with the Trans-Impedance gain set to 125KΩ*2 by an iFET ratio of 2 resulting in the same iPort scale as the previous figure 27.

Differential CiTIA used as a modulator

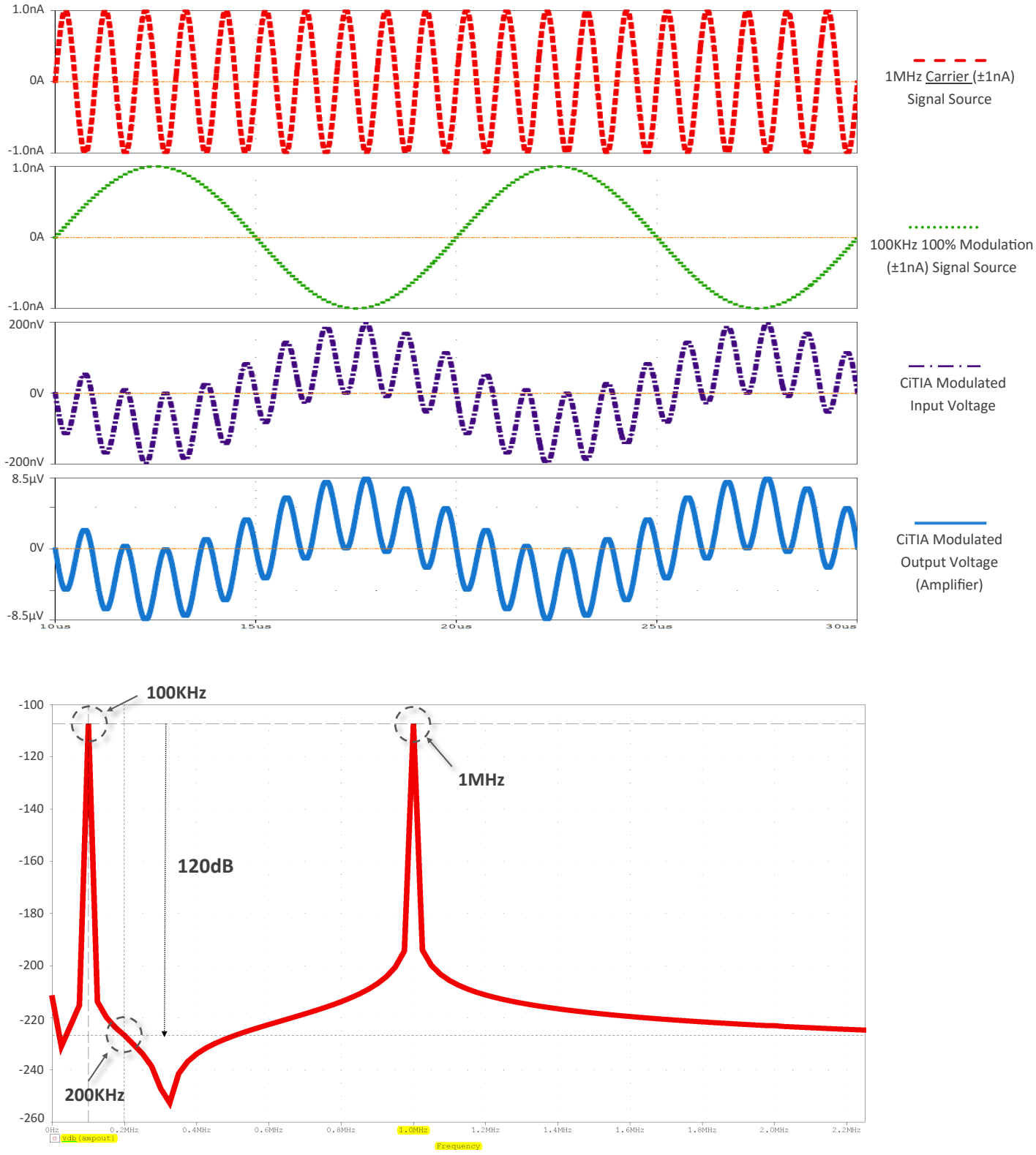

Figure 29. Differential CiTIA ***Intra-Harmonic Distortion*** from a 100% Modulated Signal = 100KHz on a Carrier = 1MHz, R_{in}=100Ω

CiTIA performance, gain, and frequency characteristic plots

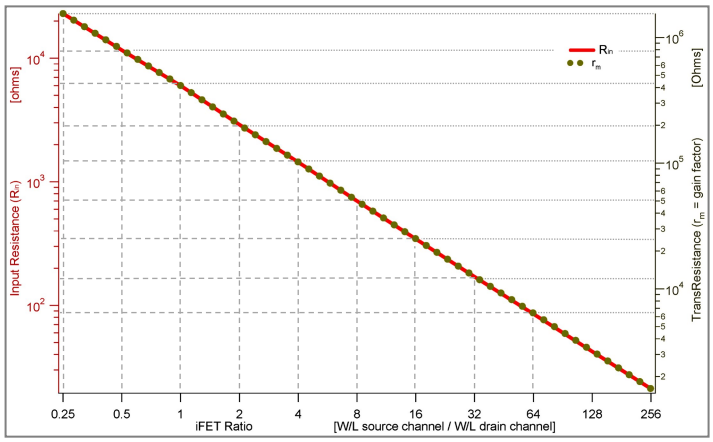

Figure 30. CiFET input resistance R_{in} (real impedance) and transResistance r_m vs. W-L ratios

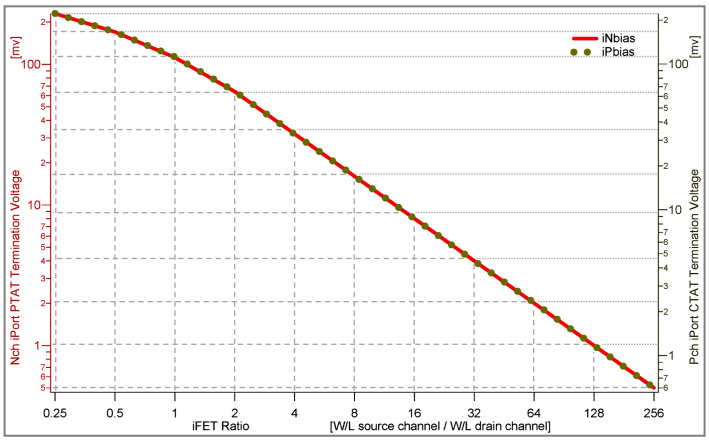

Figure 31. CiTIA iPort termination voltages to respective power rails as a function of iFET ratio

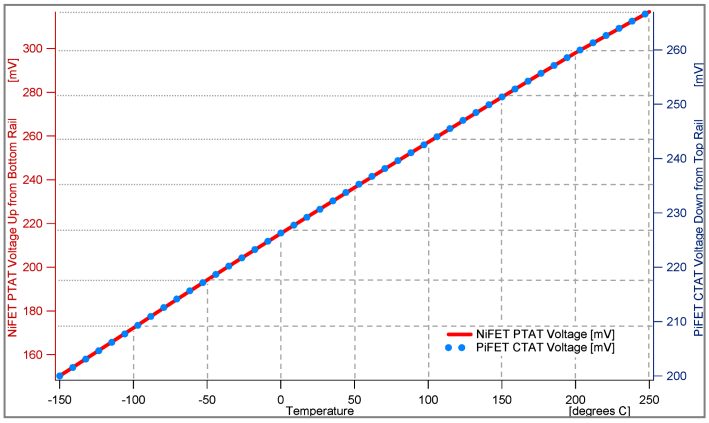

Figure 32. CiTIA iPort termination voltages as a function of temperature using an instrumentation amplifier 0.25 iFET ratio, Note: linear CiFETs operation over –150 °C to +250 °C

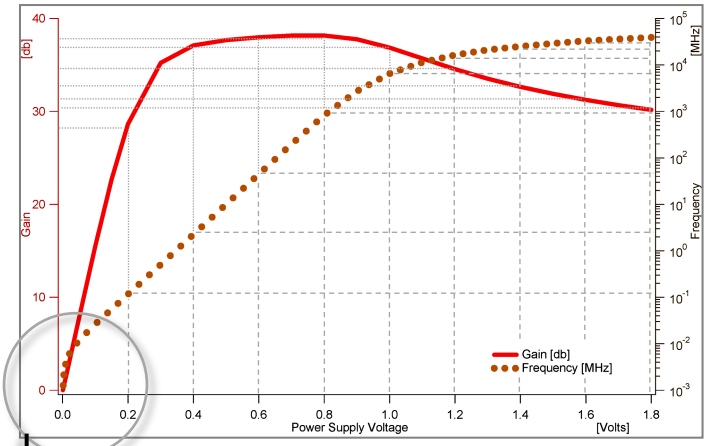

Figure 33. Gain [dB] and Cutoff Frequency [MHz] over Power Supply Voltage [V]

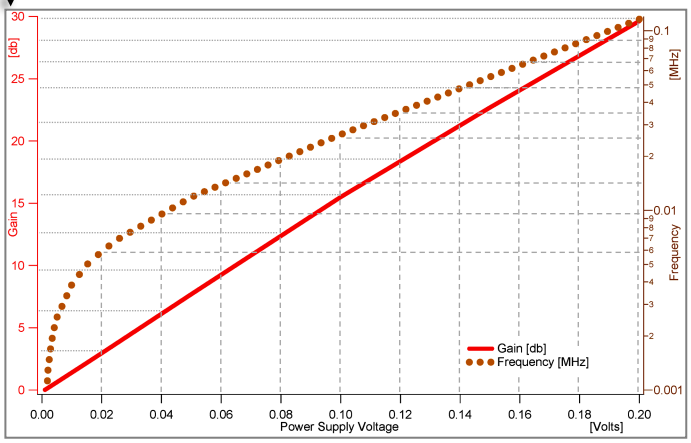

Figure 34. Gain [dB] and Cutoff Frequency [MHz] showing expanded 200mV to 10mV low Power Supply Voltage [V] range

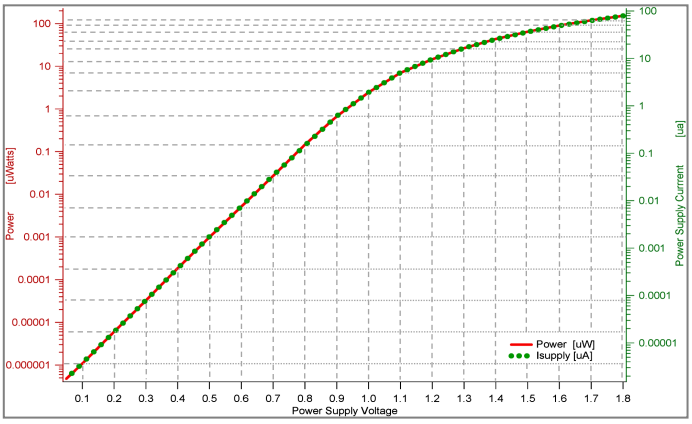

Figure 35. Power Consumption [µW] and Supply Current [µA] vs. Supply Voltage [V] for self-biased differential CiTIA

Input resistance, open-loop trans-impedance gain, phase, and noise over frequency

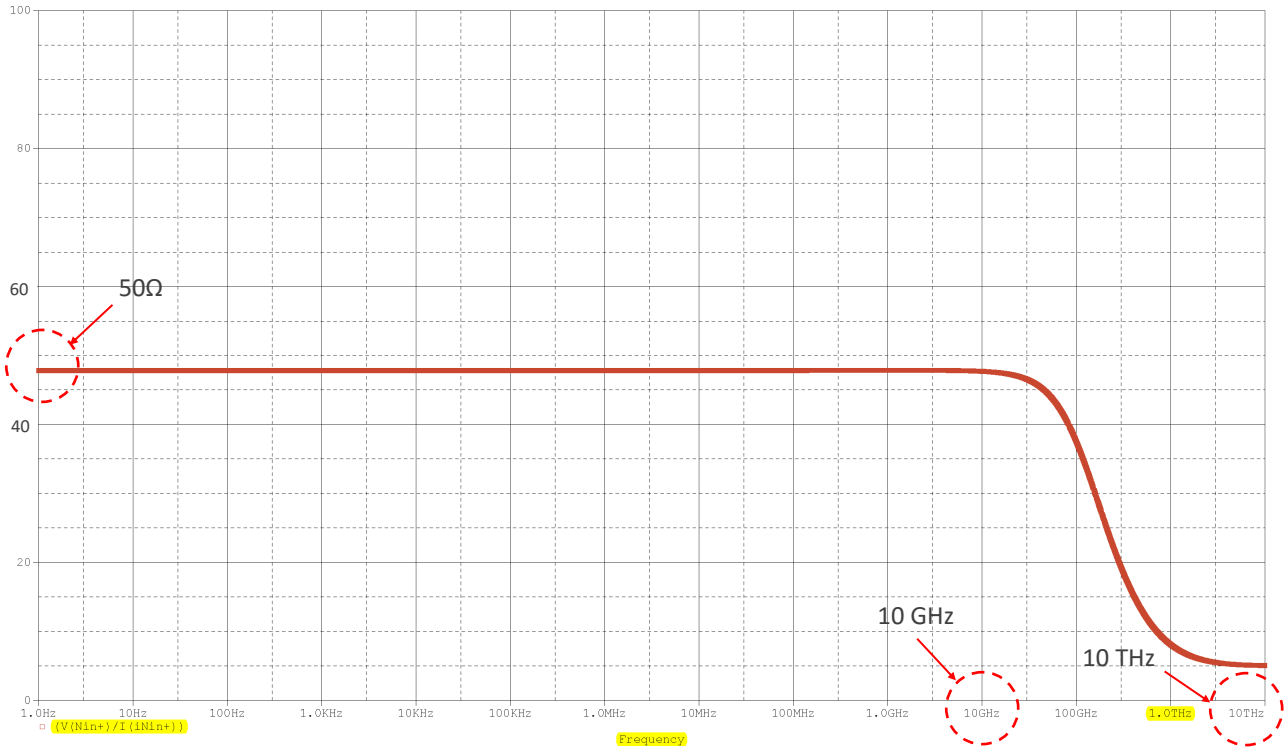

Figure 36. Differential 50Ω CiTIA input impedance over ~100GHz bandwidth for LNA applications

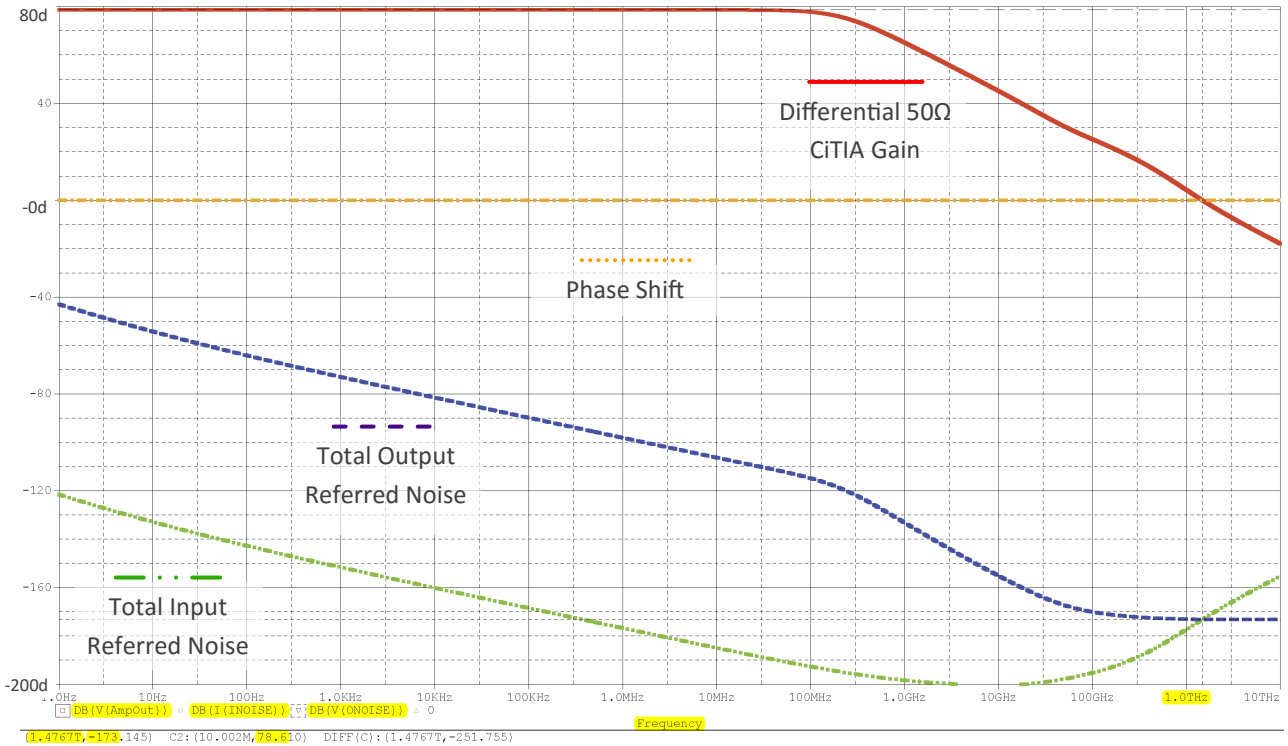

Figure 37. Frequency dependence of 50Ω differential CiTIA gain, total input and total output referred noise, with phase vs frequency

Extended-gain multi-stage full-differential CiTIA options

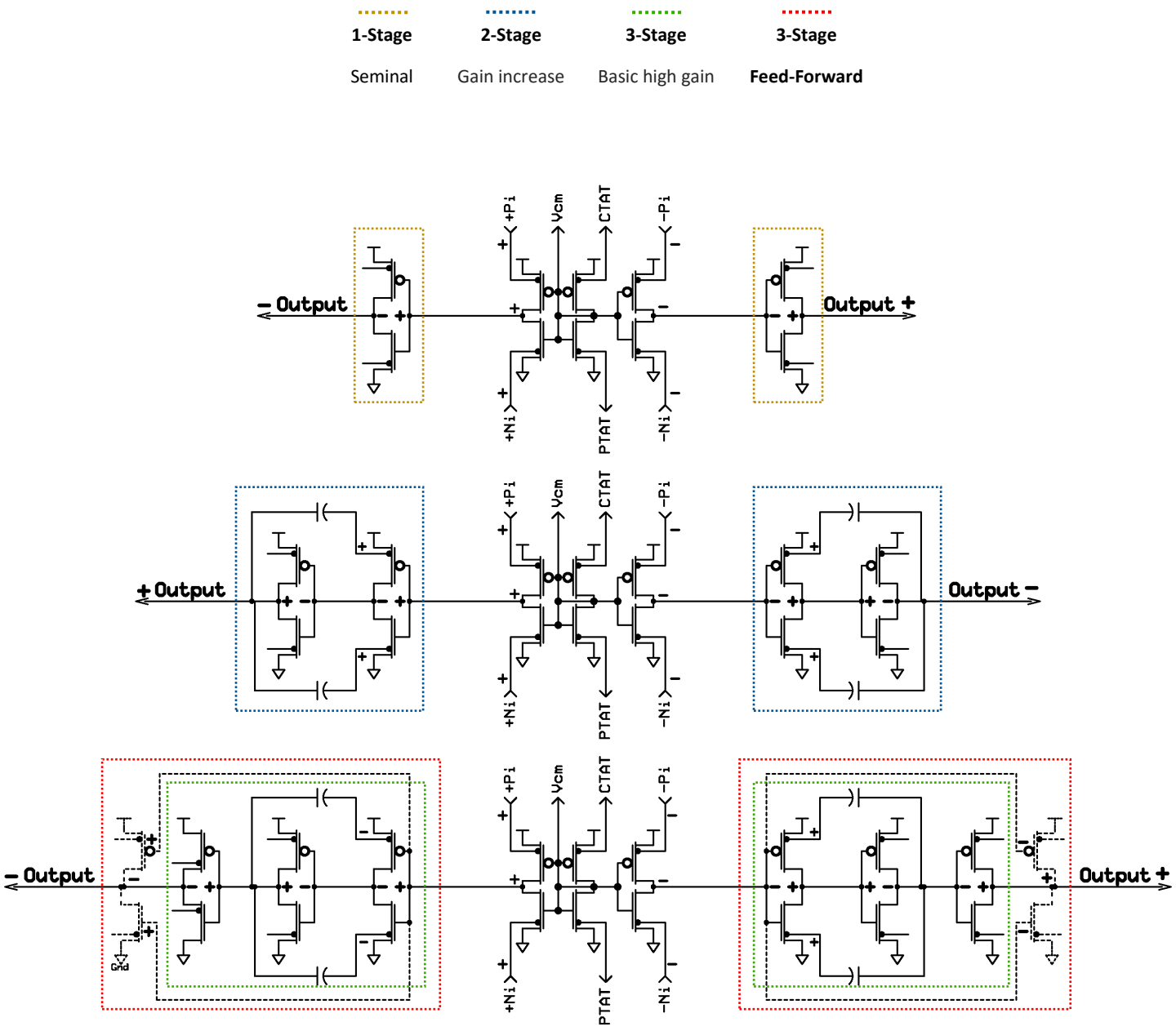

Figure 38. CiFET Multi-stage differential TIA schematics for added trans-impedance gain to a trans-impedance input stage

As with an Op Amp, utilization of a high gain trans-impedance amplifier normally includes feedback and considerations for offset correction. The capacitive feedback shown provides roll off to stabilize closed loops.

CiTIA additional application examples

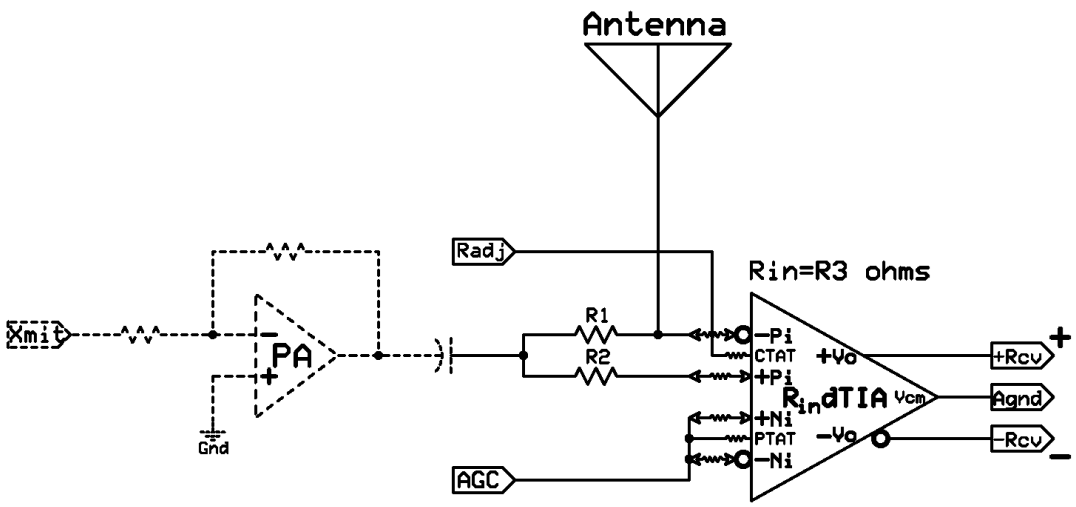

Figure 39. Enhanced full-differential CiTIA Isolator from Figure 2 employing the unused iPorts to function as R_{in} trim and/or variable gain

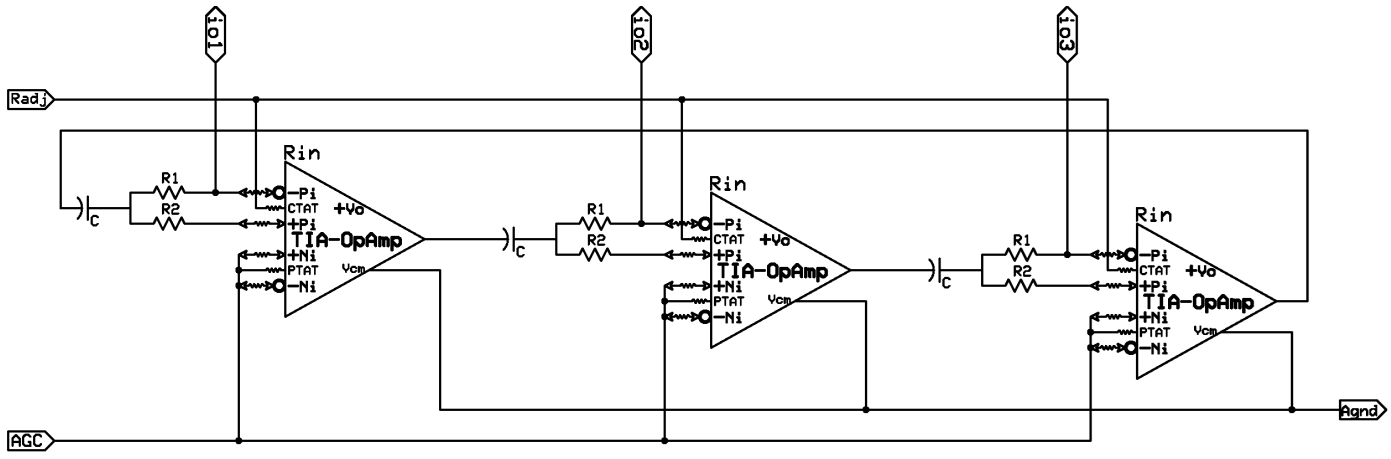

Figure 40. Example configuration of CiTIA Circulator having interchangeable Transmit, Antenna, & Receive signal ports along with a Rin trim and AGC gain control ports — where a CiFET Op Amp implementation of the PA in Figure 2 is merged into a differential CiTIA

CiTIA additional application examples

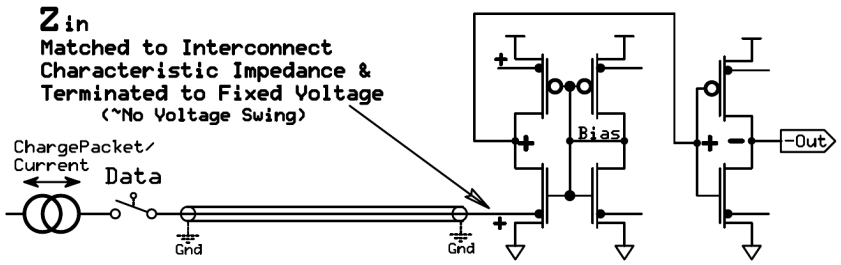

Figure 41. Example configuration of CiTIA transmission line / bus wire receiver. Multiple inputs can be summed by wire-OR connections or routed to the other iPort.

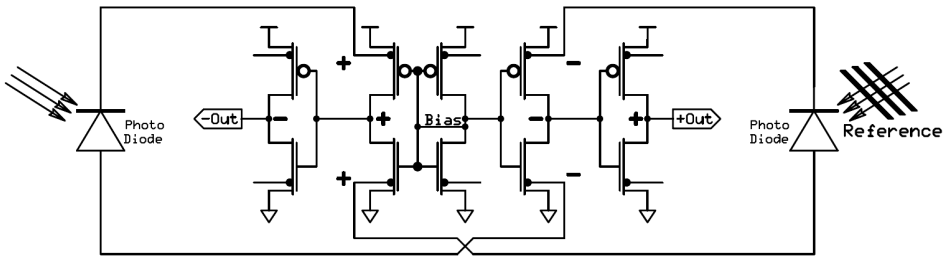

Figure 42. Example configuration of CiTIA fiber-optic receiver

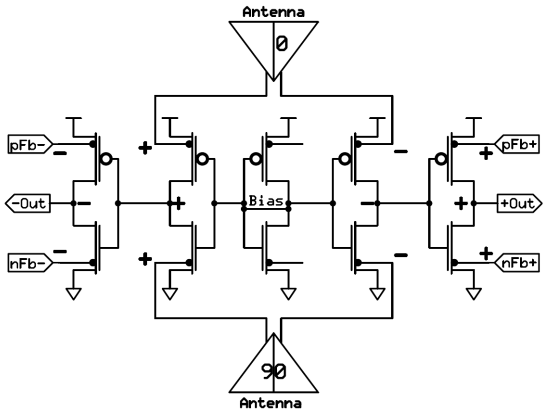

Figure 43. Example configuration of a versatile CiTIA dual additive antenna LNA with added gain and filter port / feedback access

Additional information for low noise trans-impedance amplifier (CiTIA)

Low power supply voltage restrictions in nanoscale (sub-28nm) integrated circuit processes limits the maximum signal swing to a much smaller number than most analog designers are accustomed to. Therefore, with a reduced signal, the noise must be equally reduced in order to maintain the required signal to noise ratio. It is imperative that noise issues be minimized.

Additionally, power supply fluxations are addressed by keeping analog signals biased away from the power supply near the power supply midpoint where analog signals can maximally swing without pushing into either power rail, where noise and distortion are pulled into the analog signal path. Also, differential techniques effectively double the analog signal swing headroom.

Process parameter variations including differential output voltage offsets may be sampled out during the process of centering the analog operating point near mid-supply voltage, where gain and symmetry are maximized while minimizing power supply noise injection. If cancellation of offset is required, the CiTIA based input amplifier will naturally accept offset correction inputs in the form of current or voltage from a control loop which can achieve:

- Internal input voltage bias point is self-biased to approximately ½ the input voltage "sweet spot,"
- Gain and drive symmetry are maximized,
- Offset and 1/f noise are set to zero,
- Process variations are canceled.

These can be consistently optimized with a calibration loop as required, allowing the circuit to be very exact & stable.

Virtual Ground Reference

As in all Op Amp applications, analog signals are referenced to some "Virtual Ground" reference. Even though this virtual ground may not be an actual input or output signal, it relates to the peak range that these analog signals reach. Careful consideration must be taken to not clip these signal swings against a power supply rail. This configuration uses the same output virtual ground reference that is used for the input and output of CiFET Op Amps. This analog virtual ground can be connected to either the input virtual ground or the output virtual ground reference of various CiFET based circuits, that in effect is the analog system virtual ground which is the optimum voltage for speed, gain, symmetry, and noise rejection.

Self-Biased Properties

The CiFET partially accomplishes high-gain with self-cascoding properties similar to a cascoded pair of transistors, yet without extra voltage biasing circuitry. Passing the same current through different W/L channel strengths force ratioed channel current density differences which, in turn, bias the constituent gate to channels and sum up to force the low impedance mid-channel iPort and drain output voltages. Instead of setting the gate voltage to calibrate a current, the CiFET current forces precise repeatable gate-to-source voltages. These voltages can be similarly used like a differential pair of transistors. The same current through each of these series channels is a "dual" of parallel channels used to create PTAT reference voltage generators. The voltage at the iPort (PTAT/CTAT) becomes the cascode bias supply instead of an independent gate bias voltage. Ratioed current density differences bias the CiFET.

Parasitics

Parasitic capacitance on all iPort input terminals are of no consequence because their voltages do not significantly vary at any time. This is the rationale behind using a current/charge input signal source. The corresponding low-impedance voltage output is only moderately affected by load capacitance.

Linearization

Because the CiFET pull-up and the pull-down transistors pass the same current, the complementary circuit configuration within the seminal CiFET stage cancels out its own inherent non-linarites. This enables the high exponential gain of the source channels to cancel, providing a high linearity output transfer function as exemplified in the Isolator application.

iPort Signal

A very small signal can ride anywhere on a large signal without incurring distortion as exemplified with the modulator.
Passive components such as capacitors (which are RC related to the iPort input resistance) could be utilized to create an active network for filtering (i.e. band-pass, high-pass) to amplify the select frequency of interest with tunable properties.

Trans-Impedance Amplification

Characterized as a very small current input signal (iPort current) into a relatively low fixed input resistance (Rin) & being amplified (by rm) to a larger output voltage, appearing as if the input current was passed through the relatively large (rm) resistance, forming a low impedance driven output voltage.

Trans-Impedance Characteristics
The biasing voltage, Vbias, and the iPort termination voltages are set by the combination of two factors:
1) The ratioing the complementary iFET W/L channels,
2) sizing the PiFETs with the appropriate multiplication factor that accounts for the hole-to-electron mobility differences in the same way PMOS is typically done for CMOS logic gate sizing .

Trans-Impedance Gain
Weak-inversion gain and dynamic range are exponentially generated, but are weak and slow. The CiFET is the embodiment of weak-inversion on steroids. This has been an evasive target since the exponential properties of weak-inversion were discovered and is considered the Holy-Grail of analog by many.
The trans-impedance gain rm depends on the relative channel conductance ratios, normally set by relative channel sizes primarily and not the IC process parameters, yielding a very-high degree of design portability.

Highest Gain
The CiAmp is not bounded by threshold voltages, and its highest gain is delivered when both the source and drain channels of the complementary iFETs are in the exponential sub-threshold regime. For instance, the highest gain for the 3-stage CiAmp is typically 160dB (100 Million, equivalent to ~28 digital bits) at a supply of 1.0V where the CiAmp has a bandwidth of 1GHz, while consuming about 2µA which is 2µW power dissipation.

No Crossover Distortion
There is no crossover distortion (discontinuity) on the output voltage or any of the CiTIA input current signals. Any iPort may have zero input current or be left open-circuited.

Amplifier Output Class
The CiTIA is a class AB amplifier in that the output stage maintains a small bias current. In order for the amplifier to meet the desired output voltage, the output current level is adaptive in that the available output drive current is increased by the current gain of the driving output transistor. This output can drive 10 to 100 times its bias current when needed. It's very low bias current is a result of its relatively small compound size where it can run at a high current density with very small total current drain and power consumption.

Output Drive
The output drive is in the form of a low impedance voltage source with the drive of an equivalent CMOS inverter which is very effective in driving wire capacitance loading.

Output Swing
The output swing can reach the power supply rails, but it is not recommended because being at a rail means that power supply noise is directly coupled into the analog signal path, which is a general property of any analog design. Differential signal swings enable a 2x V_{dd} dynamic range with a linear range of over 1x V_{dd}.

Low Power & High Speed
Low power operation along with high speed is due two reasons:
1) The minimum parasitic capacitance due to the attributes of the digital-like, minimally-sized transistors that make up the CiFET, and
2) having a near-maximum current density within the CiFET to charge parasitic capacitances, while keeping the total power supply current relatively small as a result of the small device sizes.
Note that high current density is set up by the CiFET channel length to be within a safe maximum level in their host IC process.

Speed
The high (or maximum) current density with a compact (or minimum) area enables exceptional (or maximum possible) speed — minimum Capacitance driven by a maximum current. Here, the analog signals do not have to transition the full power supply voltage range like a logic inverter. Speed scales proportional to ring oscillator logic speed and is potentially faster due to not having to get unglued from the power rails and operating only around the Vdd midrange where the logic signals have their maximum slope.

Speed Limitations
The CiAmp configurations are not limited in terms of speed due to velocity saturation like traditional amplifiers. The super-saturated channels transmit current predominately by charge diffusion rather than carrier transport. In other words, the electrons do not have to transverse the entire channel length, but rather have to only push on their adjacent electrons in order to knock an electron off the end of the drain channel. This high-density carrier concentration in turn provides a low output impedance, which adequately drives CiAmp loads along with any additional parasitics. The CiAmp speed scales directly with logic process ring oscillator speed.

1/f Noise
1/f noise (pink-noise) is by far the most significant noise component, especially in the super-saturated source channels where power gain is exponentially obtained. For Low-Noise-Amplifier (LNA) applications, excessively low impedance wide source channel regions provide an abundance of averaging charge carriers, which are a result of the over-threshold gate-to-channel voltage collecting and diffusing the carriers below the surface avoiding the dominant carrier trap region. In addition, the carriers do not move significantly along the surface, but behave in a manner to Newton's cradle shown in Figure 27.

Source Channel Noise
1/f noise in the voltage gain generating source channel is reduced because the self-bias scheme provides a high field strength to the source channel by its gate, forcing carriers in the channel to operate below the surface, where there is a smoother path (fewer obstructions), rather than along the surface where crystal lattice defects interfere.

Drain Channel Noise

1/f noise (pink-noise) from the output level translating drain channels is low as a consequence of the CiFET's self-biased high common gate voltage being set to near half Vdd midpoint (sweet-spot) voltage. This imposes a higher (above Vthreshold) than normal electric field applied to the entire drain channel. This biasing not only keeps the charge carriers below the surface but avoids velocity saturated channel pinch-off at the surface near the drain. This in turn unleashes speed by avoiding charge carrier transit time limiting pinch-off velocity saturation along with the noise inducing hot-carrier injection into the gate oxide. This also keeps the output resistance low in order to drive the trans-impedance amplifier voltage output.

Wide Band Noise

Wide band noise (white-noise) is always an issue in high gain, high frequency circuits. While conventional designs adjust the gate voltage to establish the operating point, CiFET designs establish the gate voltage at the optimum point (the "sweet-spot") and then selects the longer channel lengths to establish a desired operating current. This approach establishes a higher quiescent current density where the abundance of charge carriers have lower (resistance collision-generated) wide band noise.

Resistor Noise

Resistor noise is minimized because the self-bias configuration puts the iFET complementary pair at its lowest channel resistance operating point. Resistance is caused by collisions between carriers and the surrounding atoms in the semiconductor. The lower the resistance, the fewer the collisions.

Ground-Loop noise

Diminished because the analog circuit ground is "virtual" (just like in many op-amp circuits) rather than ground being one or the other power supply connections where ground currents inject voltage noise. In feedback applications, the isolated virtual ground is the desired reference for high precision closed-loop circuits. The use of "differential decoupling" (flying capacitors) offers transformer-like isolation with the compactness of integrated circuit elements.

Power Supply Noise

High common mode power supply rejection is inherent in the complementary CiFET circuit. Signals are with respect to the mid-point instead of being with respect to one of the power supply rails (similar to an Op Amp with its "virtual" ground). Power supply noise is from one rail to the other, equal and opposite in phase with respect to each other, thus canceling around the mid-point. Inputs and outputs are floating with respect to the power supply to minimize injected noise.

Coupled noise

Injected by fringe capacitance "parasitic induced crosstalk" which increases by the square of the signal amplitude. Unintended capacitive coupling with a 1 volt signal causes a lot more trouble than with a 100mV signal, by a factor of 100:1 (square law effect). The small voltage signals employed in the analog sections reduce this capacitive coupled interference substantially. Nearby digital signals will, by definition, be high amplitude (rail-to-rail). Good layout practices are still the best defense against this digital source of noise.

Virtual Inductor Application

Using a capacitor in the feedback of a trans-impedance amplifier functionally substitutes as an inductor dual. The trans-impedance amplifier with a capacitor in its feedback functions as a gyrator performing as an inductor. Because of the extremely wide bandwidth of the CiFET TIA along with the low "dual" equivalent resistance of the capacitor, the simulated inductor has very much greater quality-factor "Q" than an integrated inductor or even an external inductor. The CiTIA functions at the required frequencies required in modern systems. As an example of this, oscillators and Phase-Locked-Loops (PLL) have been fabricated and tested with numerous oscillators providing spectral purity of greater than 70-dB with operating frequencies of up to 30GHz, completely integrated in digital technologies.

Charge Mode Design

The CiTIA enables charge-mode logic (CML) digital circuits operating with fast switching current instead of voltage. The CML interconnect is speed-immune to C_{load}. Essentially inverters are the gain element which are arguably the highest gain configuration of a complementary pair of transistors. The balanced complementary nature also cancels out non-linarites.

Scalability

Since CiFET based circuits are fundamentally based on a logic inverter and operate wherever an inverter operates, yielding proportional performance, while having the portability of logic circuits. Their operation is highly scalable to IC process nodes not requiring major rework to accommodate process parameter variation, including FinFETs. However, due to their high gain and speed, careful physical layout to keep stability and performance in check. The basic iFET ratios remain constant.

Summary Thoughts

The CiTIA absorbs maximum signal energy from a source and converts it to a low impedance voltage. The CiFET proposes to provide a superior signal energy gain component using a logic IC process, shifting design focus away from amplifiers and onto the surrounding circuitry. The CiFET approach empowers exceptional performance with scalability into nanoscale logic-only IC processes. As in any good analog design, good design practices need to be employed in CiFET charge-mode designs.

Note: CiFET circuits are linearized and symmetrically balanced through the use of complementary diffusion types rather than conventional analog current loading and biasing techniques.

About Circuit Seed

Circuit Seed is a new family of building block circuit designs for processing analog signals that includes a new CMOS Field Effect Transistor (CiFET) with unique properties. These designs all use 100% digital workflow components overcoming many of restrictions of traditional analog circuits. Circuit Seed is a team of highly-skilled, experienced IC designer-inventors in the areas of analog, digital, mixed-signal, and RF design.

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