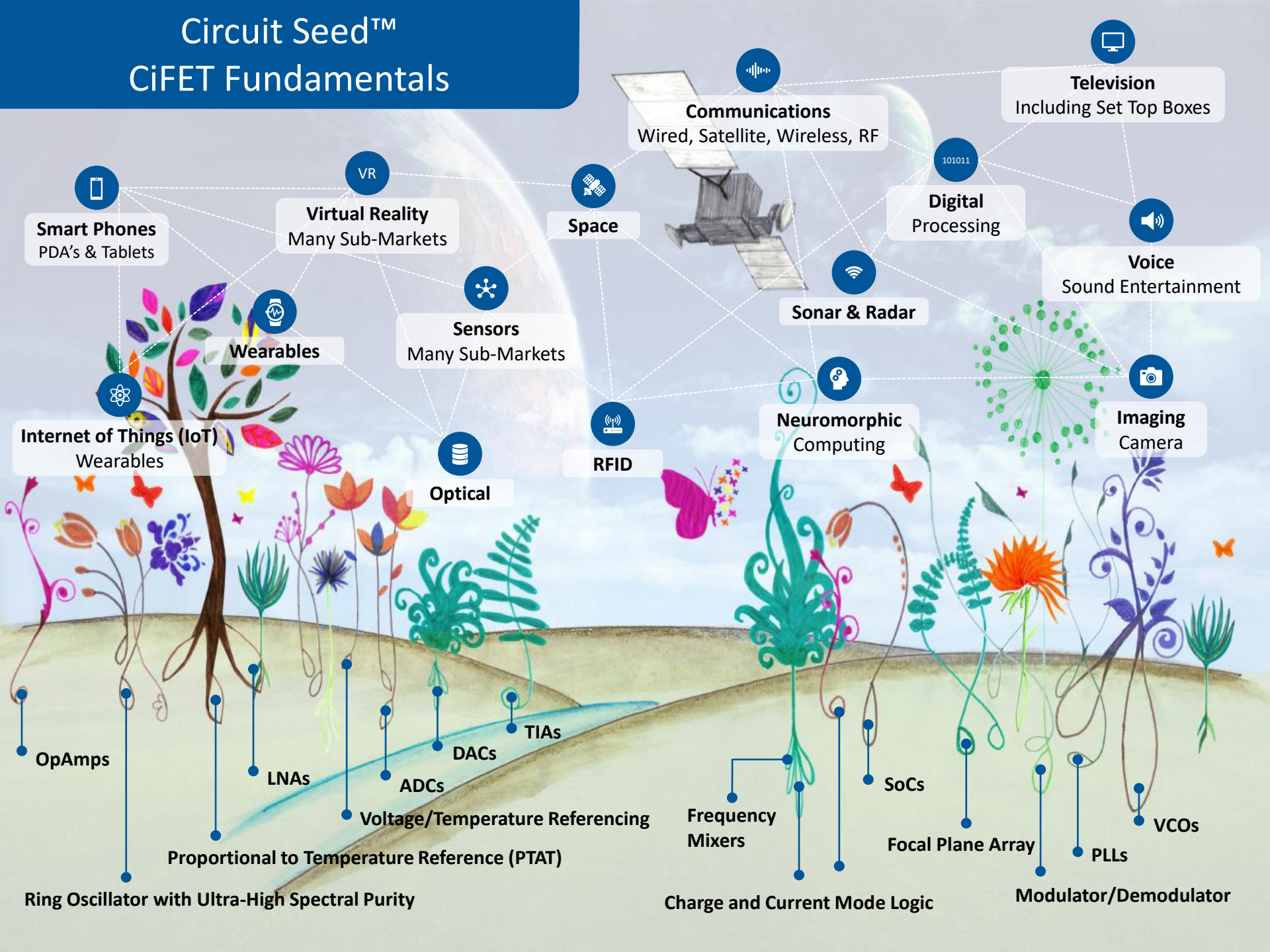
# Circuit Seed™
# CiFET Fundamentals



Circuit Seed™

Click Menu



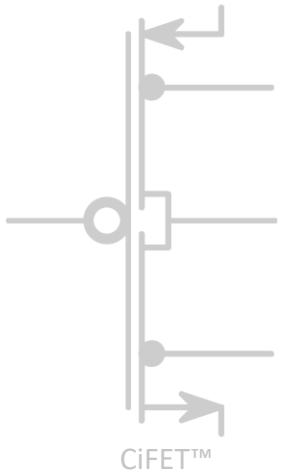
***NOTE:*** *For consistency, most results are based on a 180nm/130nm EKV simulation model. As process shrinks, performance scales with logic speed.*

# CiFET™

(Complementary Current Injection Field Effect Transistor)

The CiFET™ is a unique new logic device that performs multiple high-quality analog circuit functions simultaneously from a single fusion FET device.

The CiFET™ is new look at analog IC transistors which permit linear circuitry to be tightly coupled to microprocessors, DSP, and logic within the same digital chip. This is realized in any existing or evolving nanoscale IC process node (including 100% digital IC processes) without process extensions or modification to enable superior fully-integrated analog functionality.




The CiFET™ enables a new portable family of building block circuit designs for processing analog signals in an all digital domain -- based on a new Field Effect channel fusion for fully integrating analog functionality with unique properties while eliminating separate analog chips and external components on the circuit board. Noise is markedly reduced and sensitives considerably increased.

CiFET™ designs use 100% digital IC transistor channels to overcome many traditional analog restrictions including parametric, leakage current and temperature sensitivities, need for precision or matched transistors and current mirrors, while providing ultra-linear response over an extended dynamic range along with the capability of operating at low supply voltages below 800mV with low power consumption at any threshold voltage.

# The Industry Problems in Emerging Nanoscale IC Process Nodes

**Power supplies are limited to about 800mV forcing:**

- Analog dynamic range limited to less than 3 decades, because:
  - Threshold voltage reduction causes insufficient transistor turn off,
  - Off-leakage currents approach analog operating currents, making
  - Leakage power increase to power dissipation limits, while

**Analog voltage swing is limited to hundreds of mV (threshold to linear saturation)**

- Signal to noise margins vanish;
- Analog reliability and yields become an insurmountable limit, because:
  - On-Chip-Variation of a single transistor changes analog signal voltages up to ~40%,

**Only one-sized transistor is available (process nodes are tuned to making only one size)**

- Short channel shunting reduces intrinsic gain ($g_m$*$R_{out}$) to 1
- No analog IC process extensions will be available
- Low yields when analog is included on the chip

# CiFET™ Fundamentals

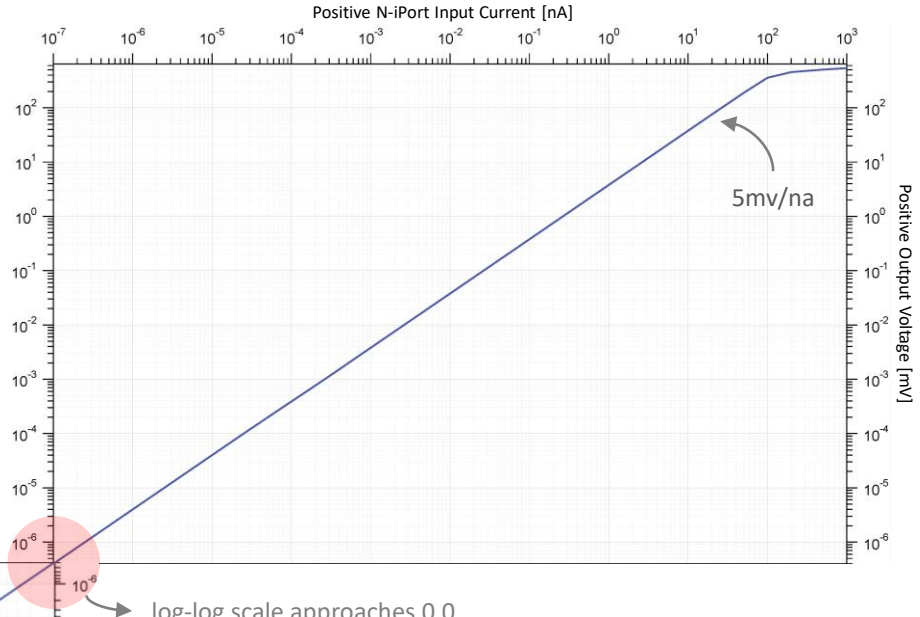
A fusion of field-effect channels provides unprecedented analog performance in any logic IC process or technology which improves with IC process shrink

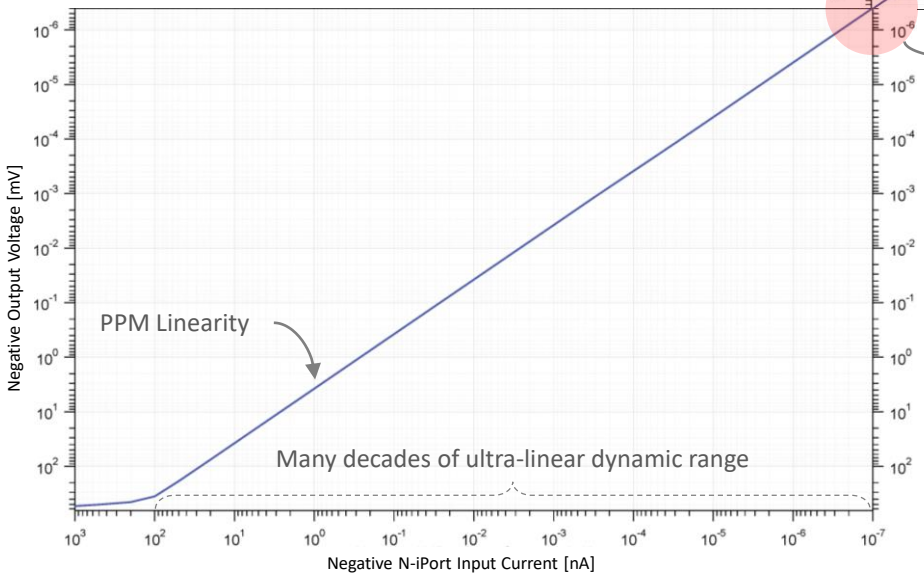
# CiFET™ Ultra-linear high Trans-Impedance Gain

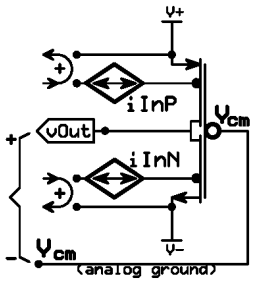
Primary CiFET™ asset is ultra-linear high Trans-Impedance Gain over an extreme dynamic range

**N-iPort {or P-iPort} Input Current [nA] controls $V_{out}$ [mV]**

- Non-inverting functionality
- Bi-directional input current
- Precise Symmetry
- Zero input current valid
- No crossover distortion
- PPM (>20-bit) linearity
- Ultra-Low Noise
- Record-setting Dynamic Range
- ~Rail to Rail Output
- 4-Quadrant functionality with
  - Full-differential implementation
- Current inputs locally terminated for
  - Ground noise tolerance



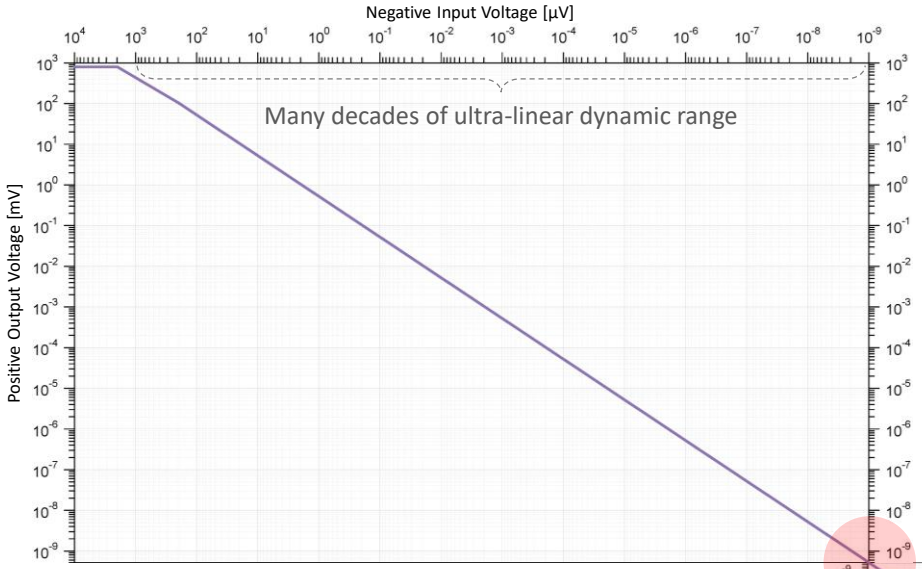




- P-iPort functions precisely identical to the N-iPort
- Using both iPorts algebraically sum independent inputs
- Both iPorts are non-inverting
- Multiple input currents yield their wire-OR sum
- Unused iPorts are left open-circuited (= zero input)

# CiFET™ high ultra-linear Voltage Gain

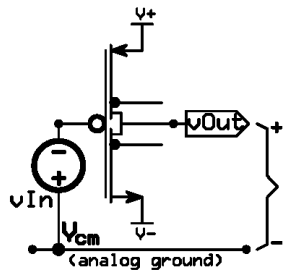
The CiFET™ produces high ultra-linear Voltage Gain over an extreme dynamic range



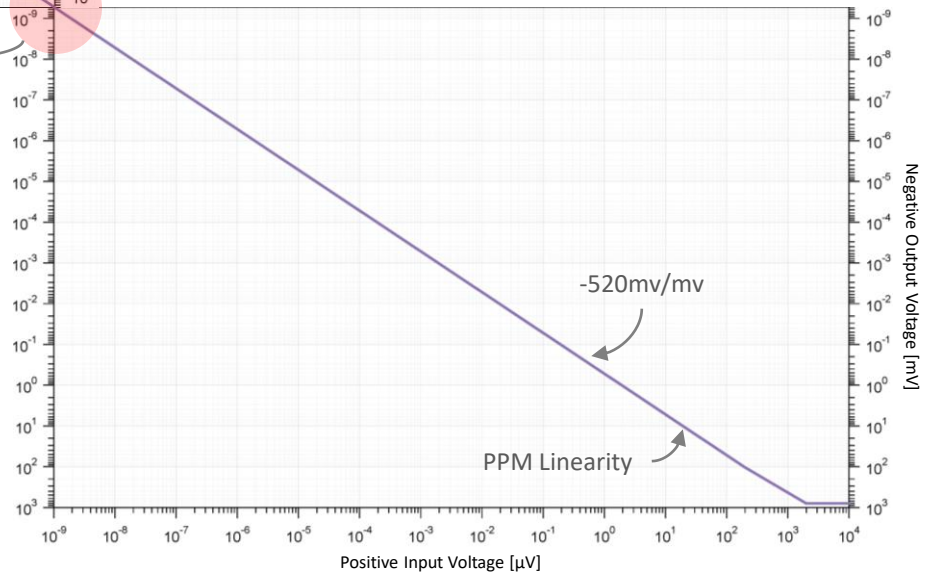

**Gate Input Voltage [µV] controls $V_{out}$ [mV]**

- High input impedance
- Low output impedance
- High voltage gain
- Inverting functionality
- Bi-directional input voltage
- Precise Symmetry
- Zero ($V_{cm}$) input voltage valid
- No crossover distortion
- PPM (>20-bit) linearity
- Record-setting dynamic range
- Ultra-Low noise
- ~Rail to Rail Output
- Operates concurrently with iPort current inputs

log-log scale approaches 0,0

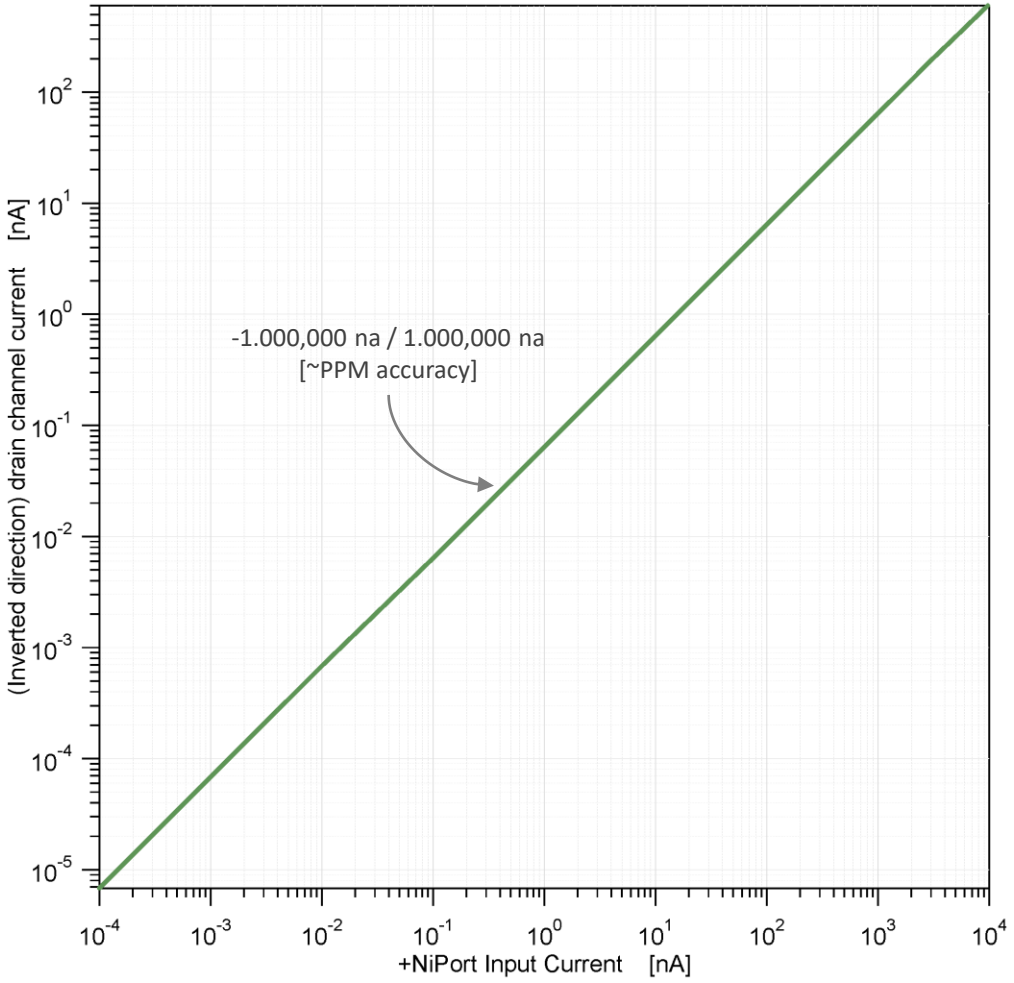


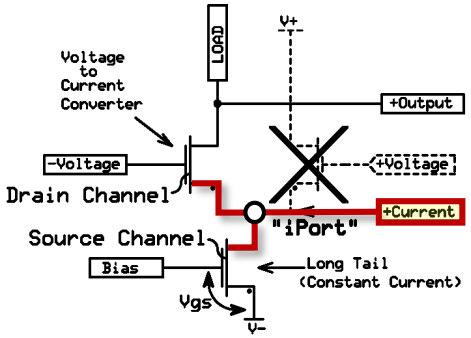

- Voltages swing about $V_{cm}$ (~$V_{dd}$/2) where
- noise coupling is symmetrically cancelled
- Functionality also includes either or both iPorts
- All voltage and current input signals algebraically sum
- 4-Quadrant functionality
- Full-differential implementation optional

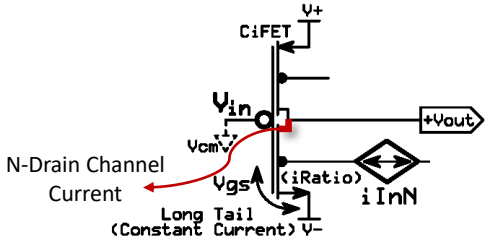


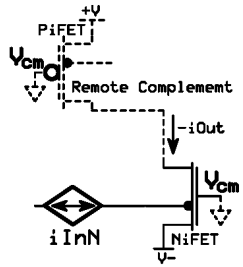
# Precision CiFET™ Current Inverter

Reminiscent of a current mirror, but input current is precisely ***inverted*** with PPM (20-bit equivalent) accuracy
(CiFET™ bias current included here translates from one to the opposite CiFET™ polarity and the bias can be subtracted out if necessary)



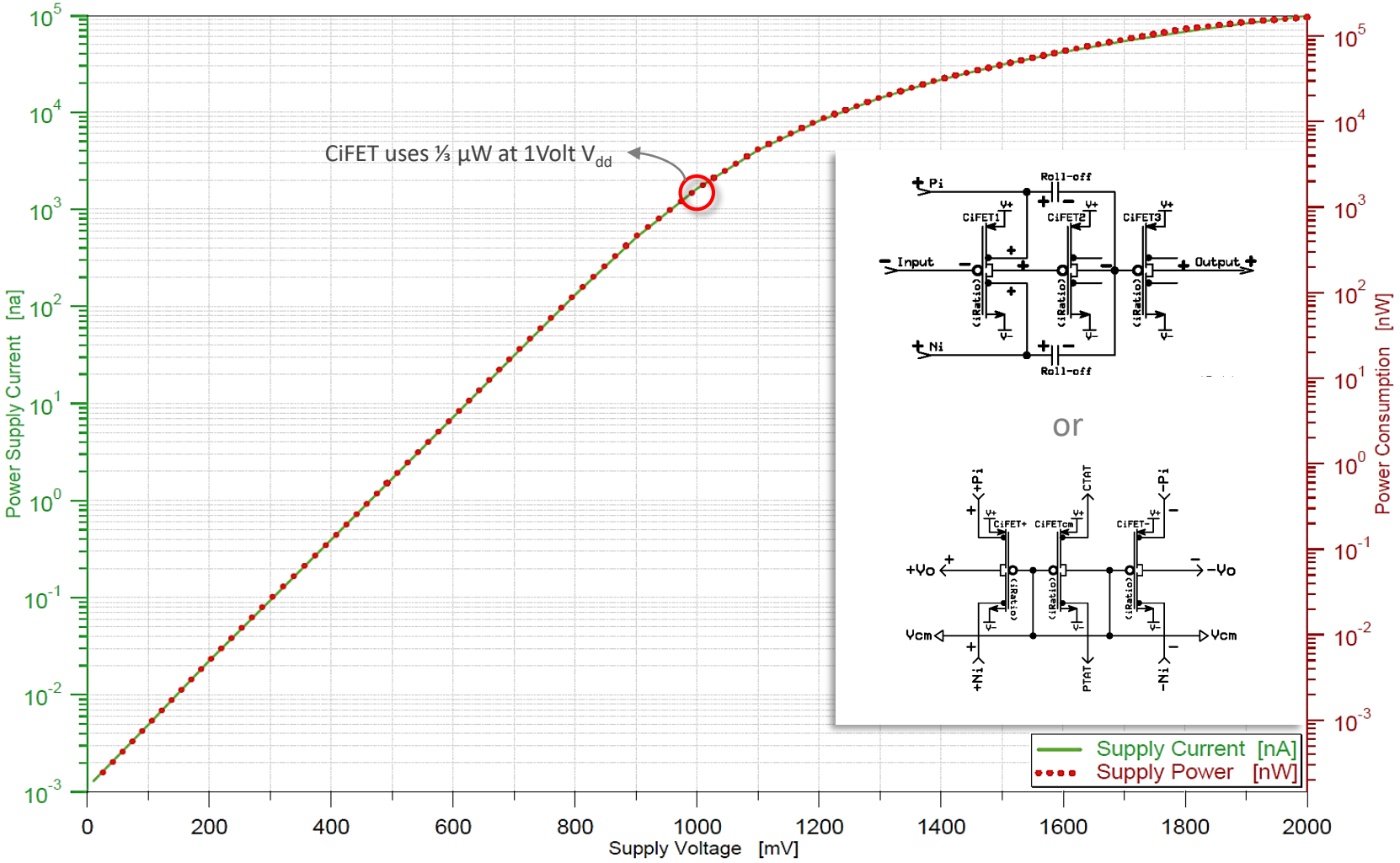



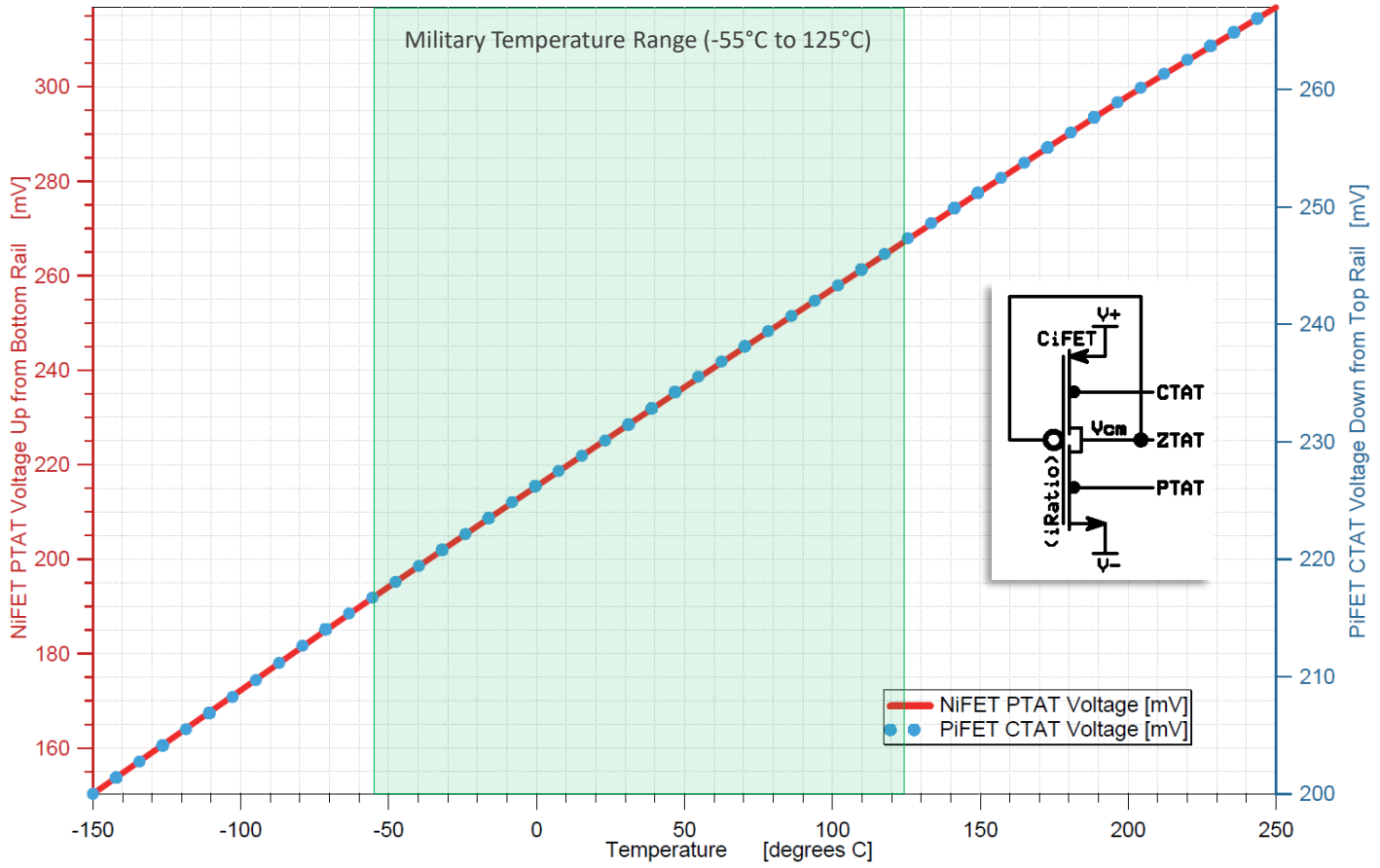
# CiFET™ Amplifier

Triple CiFET™ Amplifier Supply Current & Power vs $V_{dd}$



# Temperature Measurement & Common-Mode Reference Generator

Self-Biased precision CiFET™ PTAT (Proportional-to-Absolute-Temperature) and CTAT (Complement-to-Absolute-Temperature) iPort voltages are set by iRatio, have precise linearity, and are essentially independent of semiconductor property variations over an extended temperature Range. The ZTAT (Zero-to-Absolute-Temperature) terminal generates a self-biased Common-Mode analog ground (Vcm) located ~mid supply voltage where maximum analog voltage swing is available for bidirectional analog signals.



# CiFET™ iRatio

Gain and other properties are regulated by physical iRatio device sizing
taking the pressure away from semiconductor parameters and temperature

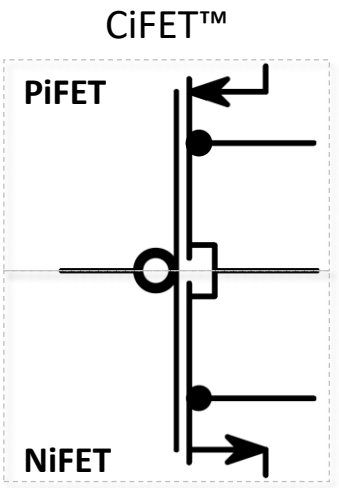
# iRatio & cmRatio

An iFET (current injection Field Effect Transistor) is a MOSFET that has an extra diffusion located in its conduction channel, providing access to channel current flow. The iRatio (current density ratio) represents relative iFET channel strength ratio (Source Channel strength / Drain Channel strength). More specifically, it is charge density ratio between operating iFET channels.

Similar to a CMOS Inverter, the CiFET™ (Complementary iFET) is a complementary pair of iFETs. The complementary P-iFET is normally set to the same iRatio, but both P-channels are wider by the cmRatio (common-mode Ratio) which is used to approximately balance the P to N mobility differences. The cmRatio centers analog output voltage signal swing near half-way between the power rails and forms a common-mode voltage ($V_{cm}$) as analog ground. This enables maximum symmetrical dynamic range which tends to have complementary power supply noise cancellation while nullifying nonlinear harmonic terms in the output.

The cmRatio (the P-to-N ratio of a CiFET™) is a self-generated common-mode analog ground voltage ($V_{cm}$) that is formed by connecting the drain-to-gate of a replica CiFET™ making the $V_{cm}$ adapt to prevailing semiconductor parameters.

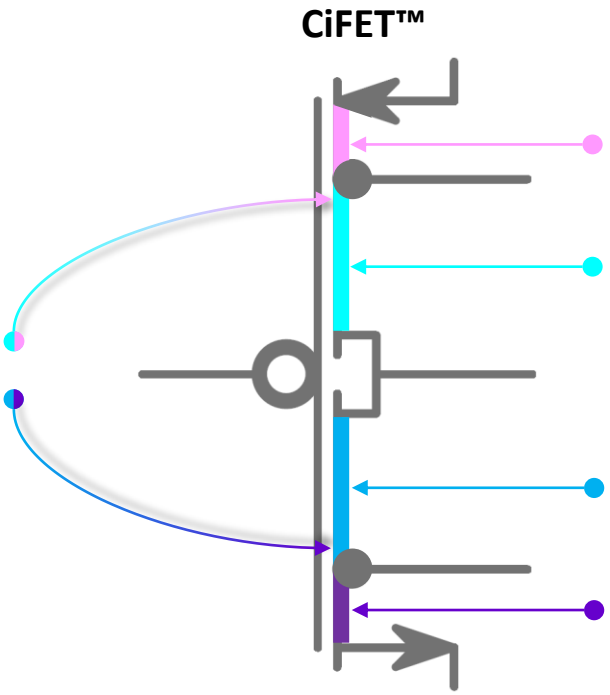
One other consideration in channel sizing is limiting worst-case pass-through (totem-pole) current in order to operate the CiFET™ within maximum allowed DC current pass-through inside the transistors and related contacts and consideration of local heating and power-speed trade-offs.



# CiFET™ Sizing Examples (iRatio & cmRatio)

Parameterized CiFET™ channel sizing in terms of iRatio and cmRatio are indicated for each CiFET™ channel.

$$\boldsymbol{cmRatio} = \frac{P\text{–}iFet\ Width}{N\text{–}iFet\ Width}$$




$$\frac{W = [P\text{–}Source\ Channel] * [Source\ Multiplier]}{L = [P\text{–}Source\ Channel\ Length]}$$

$$\frac{W = [P\text{–}Drain\ Channel] * [Drain\ Multiplier]}{L = [P\text{–}Drain\ Channel\ Length]}$$

$$\frac{W = [N\text{–}Drain\ Channel] * [Drain\ Multiplier]}{L = [N\text{–}Drain\ Channel\ Length]}$$

$$\frac{W = [N\text{–}Source\ Channel] * [Source\ Multiplier]}{L = [N\text{–}Source\ Channel\ Length]}$$

- P-Source Channel
- P-Drain Channel
- N-Drain Channel
- N-Source Channel

$$\frac{\frac{W}{L}\ (Source\ Channel)}{\frac{W}{L}\ (Drain\ Channel)} = \boldsymbol{iRatio}$$

*Both the PiFET & NiFET use the same iRatio*

# Current Density Ratio (iRatio)

CiFET™ Current Density Ratio (iRatio) Changes Functional Properties and Applications

**25Ω LNA**
>100GHz, Rin=1/16KΩ, Power=11.7µW, $r_m$Gain=80dB

**50Ω LNA**
>100GHz, Rin= ⅛KΩ, Power=11.6µW, $r_m$Gain =85dB

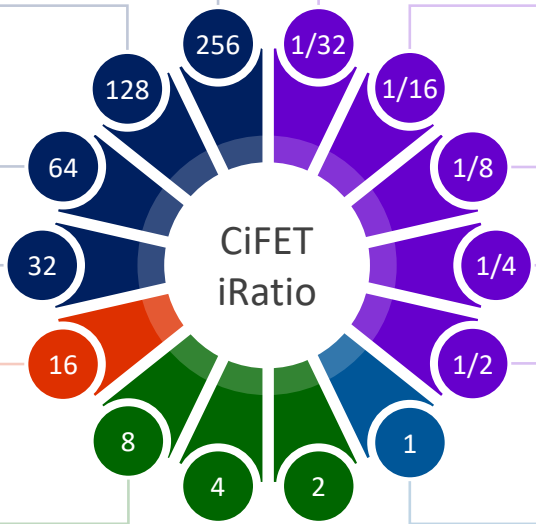
**100Ω LNA (RF LNA)**
>100GHz, Rin= ¼KΩ, Power=11.5µW, $r_m$Gain =91dB

**200Ω LNA**
100GHz, Rin= ½KΩ, Power=11.1µW, $r_m$Gain =98dB

**500Ω LNA (Transmission Line Receivers)**
80GHz, Rin=1KΩ, Power=10.7µW, $r_m$Gain =104dB

**Low Input Resistance TIA**
75GHz, Rin=2KΩ, Power=10.3µW, $r_m$Gain =110dB

**TIA (General Purpose Sensor)**
60GHz, Rin=4KΩ, Power=9.9µW, $r_m$Gain =117dB




**Ultra-High Gain Amplifier**
300MHz, Rin=350KΩ, Power=930nW, $r_m$Gain =153dB

**High Gain Amplifier**
1.4GHz, Rin=200KΩ, Power=935nW, $r_m$Gain =148dB

**High Voltage Amplifier**
3.3GHz, Rin=125KΩ, Power=7.6µW, $r_m$Gain =143dB

**General Purpose High Voltage Gain Amplifier**
50GHz, Rin=75KΩ, Power=9.7µW, $r_m$Gain =138dB

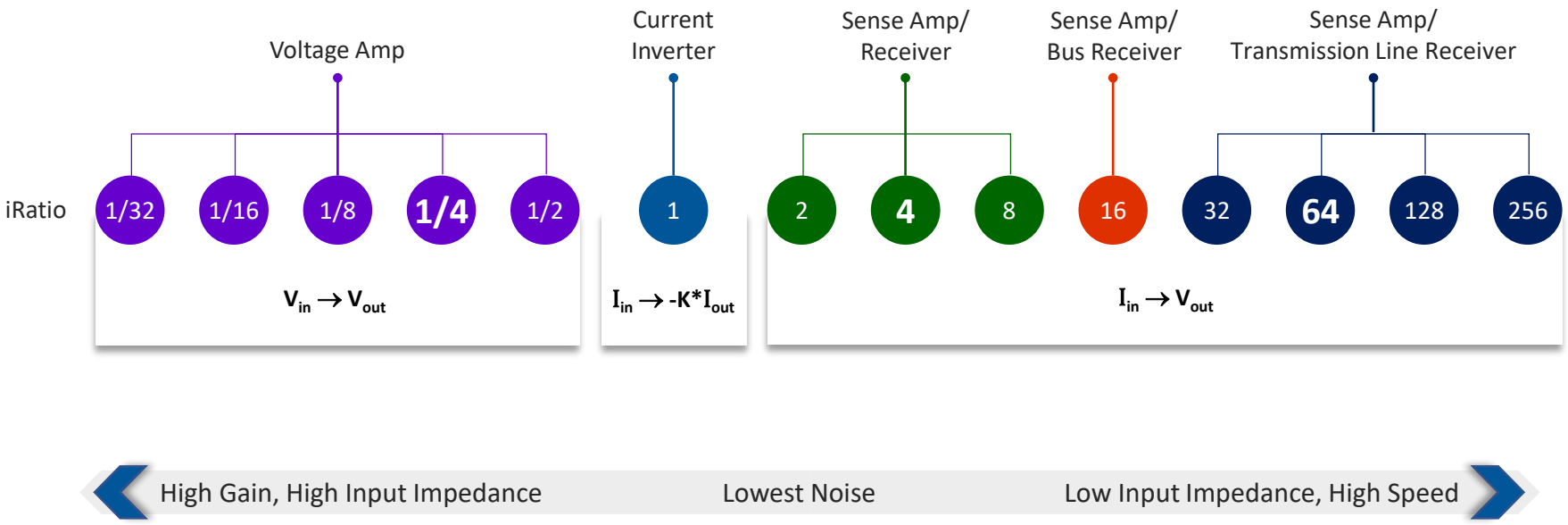
**Low Voltage Gain**
75GHz, Rin=50KΩ, Power=9.8µW, $r_m$Gain =133dB

**Minimum Area**
100GHz, Rin=12KΩ, Power=9.8µW, $r_m$Gain =119dB

**High Input Resistance TIA**
75GHz, Rin=8KΩ, Power=9.8µW, $r_m$Gain =124dB

# Current Density Ratio (iRatio)

CiFET™ Current Density Ratio (iRatio) Changes Functional Properties and Applications



**Circuit Seed designs optimally operate in logic processes from 180nm down to 5nm**
CiOpAmp™ Power Supply ($V_{DD}$) = 500mV to process limit (due to the use of switches)
CiTIA™ Power Supply ($V_{DD}$) = 10mV to process limit

Recommended range for 90% of V-gain applications
Recommended range for 90% of sensing applications

| | Voltage Amplifier $V_{in} \rightarrow V_{out}$ | | | | | Current Inverter $I_{in} \rightarrow -K^* I_{out}$ | Sense Amplifier/Receiver $I_{in} \rightarrow V_{out}$ | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CiFET™ Ratio** [iRatio] | **1/32** | **1/16** | **1/8** | **1/4** | **1/2** | **1** | **2** | **4** | **8** | **16** | **32** | **64** | **128** | **256** |
| **P Source Width*** | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 2xWide | 4xWide | 8xWide | 16xWide | 32xWide | 64xWide | 128xWide |
| **P Source Length** | 2xLong | 2xLong | 2xLong | 2xLong | 2xLong | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong |
| **P Drain Width*** | 16xWide | 8xWide | 4xWide | 2xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide |
| **P Drain Length** | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong | 2xLong | 2xLong | 2xLong | 2xLong | 2xLong | 2xLong | 2xLong | 2xLong |
| **N Drain Width** | 16xWide | 8xWide | 4xWide | 2xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide |
| **N Drain Length** | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong | 2xLong | 2xLong | 2xLong | 2xLong | 2xLong | 2xLong | 2xLong | 2xLong |
| **N Source Width** | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 1xWide | 2xWide | 4xWide | 8xWide | 16xWide | 32xWide | 64xWide | 128xWide |
| **N Source Length** | 2xLong | 2xLong | 2xLong | 2xLong | 2xLong | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong | 1xLong |
| **Input Resistance ($R_{in}$)** [KΩ] | 350 | 200 | 125 | 75 | 50 | 12 | 8 | 4 | 2 | 1 | ½ | ¼ | ⅛ | 1/16 |
| **Trans-Impedance ($r_m$)** [KΩ] | 42,000 | 25,000 | 14,000 | 8,000 | 4,500 | 1,000 | 1,500 | 700 | 320 | 160 | 80 | 40 | 20 | 10 |
| **$r_m$ Gain factor** [dB] | 153 | 148 | 143 | 138 | 133 | 119 | 124 | 117 | 110 | 104 | 98 | 91 | 85 | 80 |
| **3dB Break Frequency** [Hz] | 280K | 915K | 2.9M | 8.3M | 20M | 76M | 21M | 27M | 32M | 35M | 36M | 37M | 37.5M | 38M |
| **3dB Input Ref INOISE** [dB] | -218 | -222 | -227 | -231 | -234 | -228 | -225 | -219 | -214 | -208 | -202 | -196 | -190 | -184 |
| **NiPort Voltage** [mV] | 300 | 280 | 260 | 230 | 160 | 130 | 65 | 33 | 15 | 8 | 4 | 2 | 1 | 0.5 |
| **PiPort Voltage** [mV] | 300 | 280 | 260 | 230 | 160 | 130 | 65 | 35 | 18 | 9 | 4.5 | 2.5 | 1.3 | 0.8 |
| **Intrinsic Cutoff freq** [Hz] | 303G | 1.4T | 3.3T | 5.1T | 5T | 6.5T | 16.3T | 11T | 6.8T | 3.9T | 2.2T | 1.3T | 803G | 475G |
| **Input INOISE at Cutoff** [dB] | -184 | -182 | -179 | -176 | -173 | -173 | -173 | -173 | -173 | -173 | -173 | -173 | -173 | -173 |
| **CiFET™ Current** [µA] | 775n | 475n | 4.5µ | 8.1µ | 8.2µ | 8.2µ | 8.2µ | 8.3µ | 8.6µ | 9µ | 9.3µ | 9.6µ | 9.7µ | 9.8µ |
| **CiFET™ Power** [µW] | 930n | 935n | 7.6µ | 9.7µ | 9.8µ | 9.8µ | 9.8µ | 9.9µ | 10.3µ | 10.7µ | 11.1µ | 11.5µ | 11.6µ | 11.7µ |
| **Max. Application Speed** [Hz] | 300M | 1.4G | 3.3G | 50G | 75G | 100G | 75G | 60G | 75G | 80G | 100G | >100G | >100G | >100G |

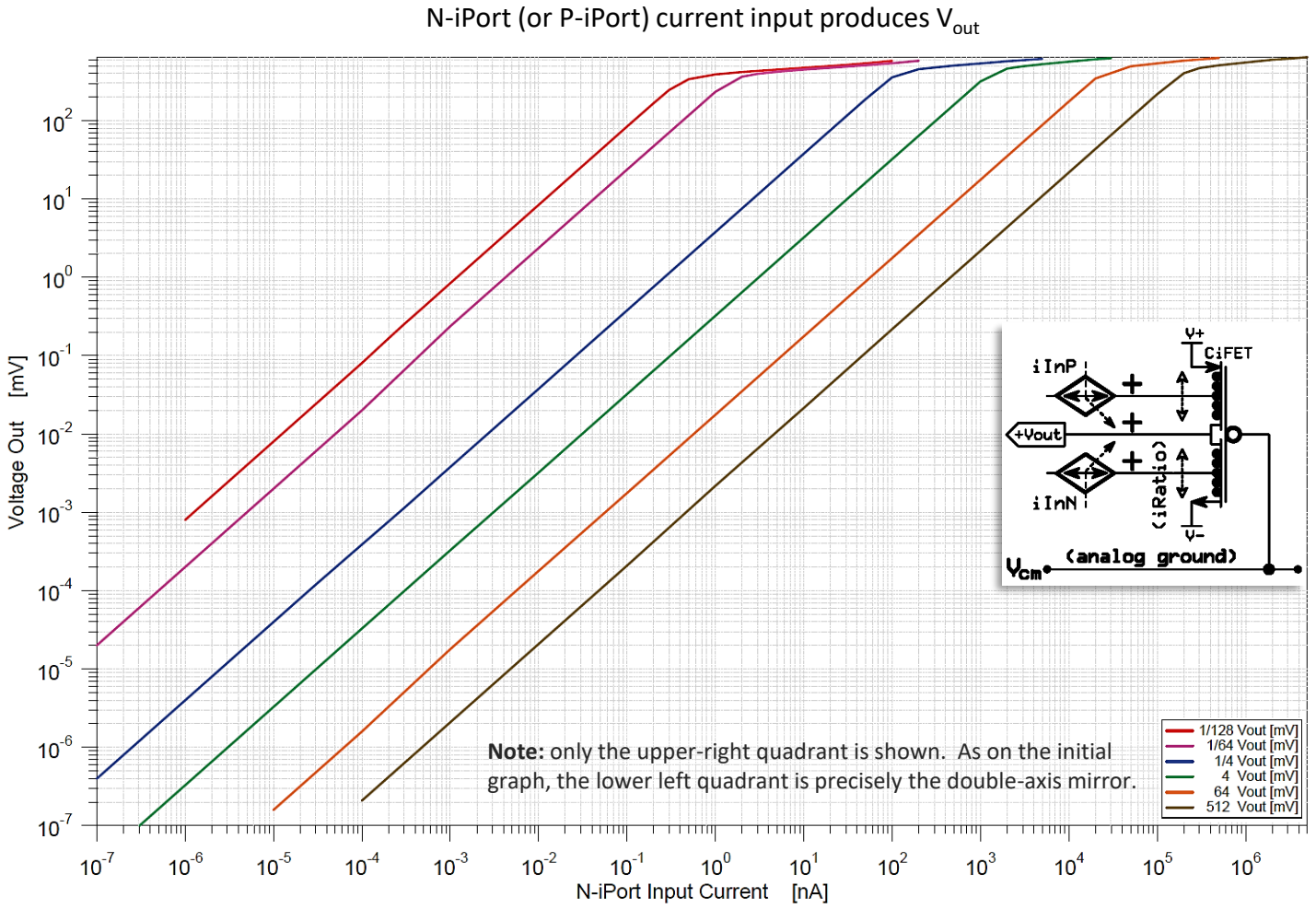
**CiFET™ Ratio** = [W/L Source]/[W/L Drain]

***Common mode ratio (P-to-N strength) =** 3 (nominal)
P channel width multiplier

**Note:** Implementation of the CiFET™ on FinFETs require all the transistors to be the same size. For the 2xWide you connect 2 FinFETs in parallel and for 2xLong, connect 2 FinFETs in series

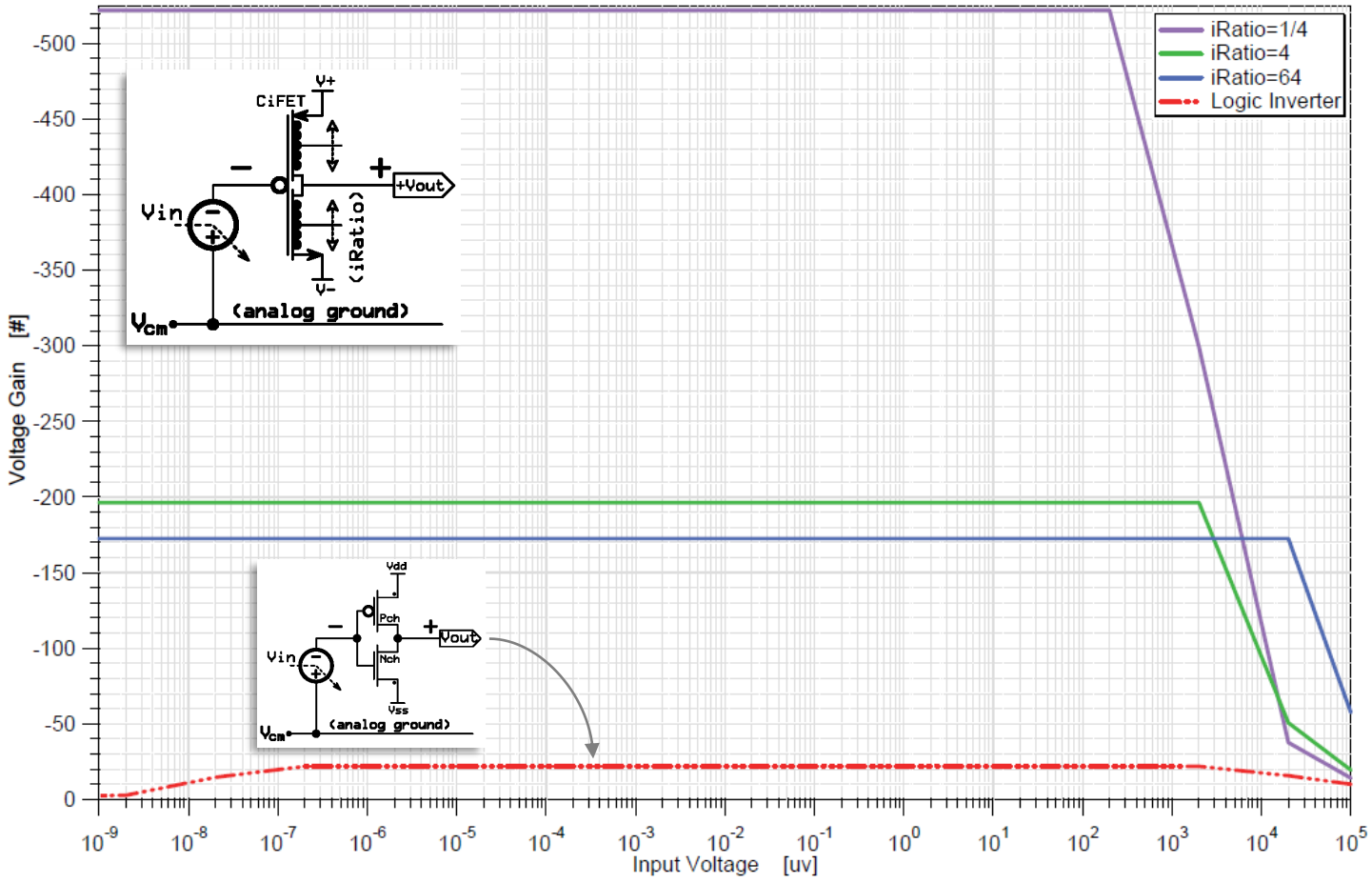
# Specifying primary CiFET™ Trans-Impedance Gain

"iRatio" (current-density ratio explained in the following section) sets the gain at design and physical layout. It is established through a pair of different channel sizes, operating on the bandgap-reference principle (explained later). Six example settings illuminate the scope of the CiFET™ Trans-Impedance gain ($r_m$) control.



# Specifying CiFET™ Voltage Gain

The voltage-gain of three primary CiFET™ examples, iRatios are compared to a logic inverter in this voltage-out as a function of voltage-in plot. The voltage gain of a logic inverter is 20 while CiFET™ voltage gain is 520 for an iRatio of ¼.



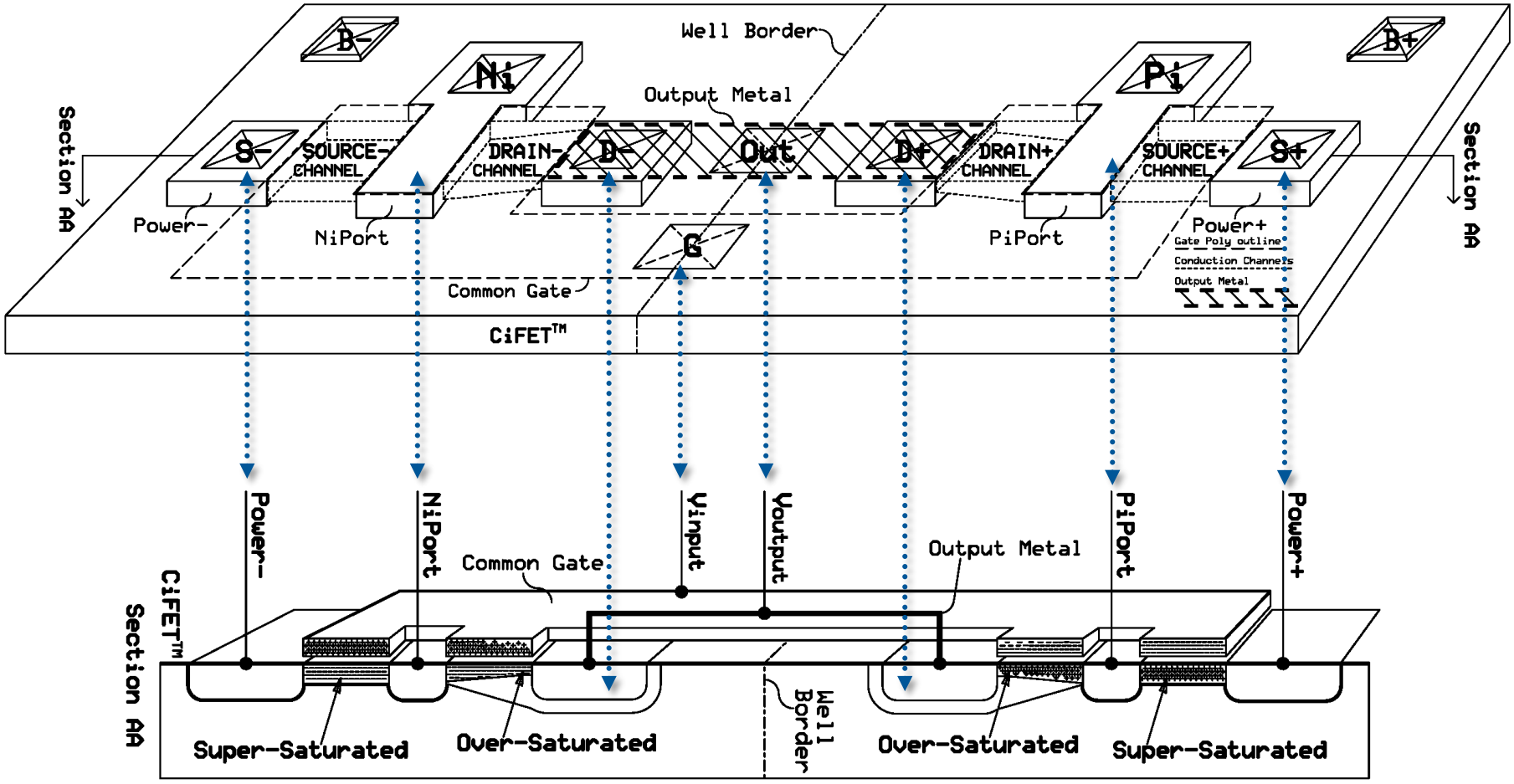

CiFET™ Voltage Gain ($V_{out}$ /-$V_{in}$) is specified by the iRatio sized channel strengths. The voltage-gain of the CiFET™ is much higher than a CMOS inverter due to the self-cascoding properties of the CiFET™ channels which provide an exponential gain boost.

# CiFET™ Structure & Operating Principles

The CiFET is a logic cell derivative that operates in the analog domain with unprecedented analog linearity, gain, stability, and low noise

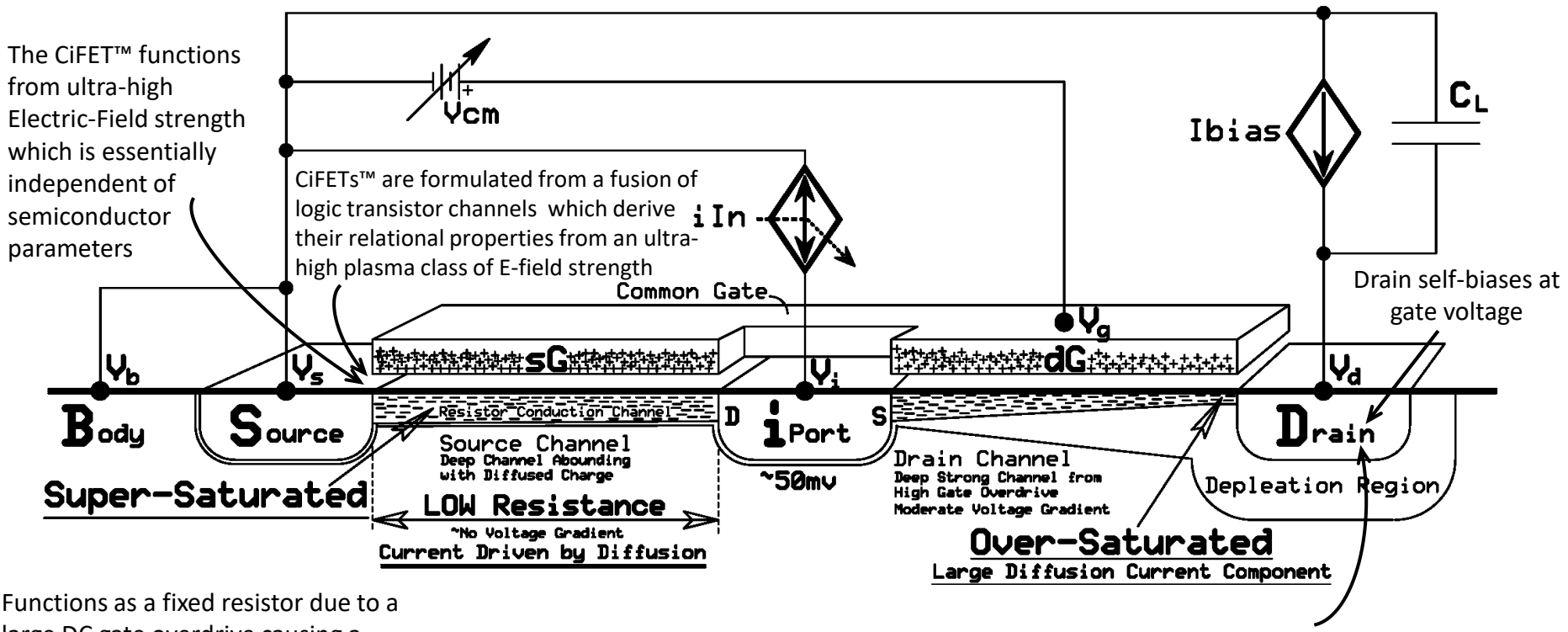
# 3-D and Cross Section CiFET™ Sketches

The CiFET™ device is constructed of native elements found in any logic-only digital IC process and does not engage IC processes extensions, which are otherwise required for analog implementation. Unlike conventional integrated circuit analog, the smaller the process node, the better the CiFET™ functions, thus CiFETs, and their circuits, are immediately portable to nanoscale and FinFETs or any other complementary FET technology (such as SiGe, Gaas, GaN, jFET, nanotubes, etc.) when newer IC process nodes are introduced. If a logic inverter works, the CiFET™ will work proportionally well.



# Channel charge distribution in a half CiFET™ device during biased operation

**3-D Cross-section Vcm biased half-CiFET (iRatio = 1)**




Functions as a fixed resistor due to a large DC gate overdrive causing a super-saturated channel

Since the CiFET is a current-mode device, the saturated nomenclature takes its que from BiPolar transistor saturation instead of MOSFET pinch-off

Note: Although the channels are actually very thin, they are drawn thicker to express their relative carrier count

CiFET™ Drain voltage swings about the self-biased DC Gate voltage ($V_{cm}$), causing diffusion channel conduction which seizes exponential gain properties with low output resistance. As voltage along the drain channel decreases, E-field driven current decreases and diffusion current increases promoting exponential gain domination. The other complementary CiFET™ half linearizes the transfer function by cancelling out harmonic terms.

Lower iRatio™ increases iPort voltage, which in turn decreases voltage along the Drain channel to further boost exponential-gain charge-diffusion operation.

Conventional analog requires long channel pinch-off regions to provide the high output resistance needed for high $g_m*(R_{out}||R_L)$ analog gain. Nanoscale transistors come in one size with a short channel which severely limits intrinsic gain to 1 at 5nm.

# CiFET™ is a Double-Layer Ultra-High Electric Field Enabled Device

Note that the gate to channel voltages bias at their maximum common-gate to channel voltage which is maximally above the normal analog threshold voltage $V_{th}$. In a nanoscale IC process, 1 volt at the gate across 50 angstroms (high K gate oxide insulator for 11nm transistor) is an electric field strength of 200 million volts per meter – lightning strikes at 3 million volts per meter.

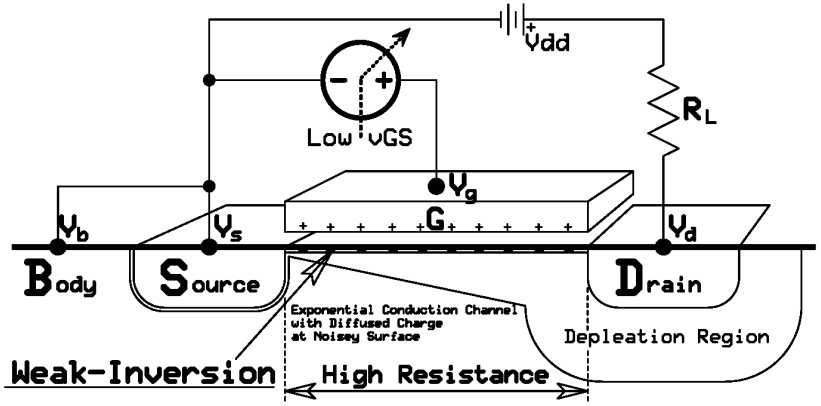
The CiFET™ takes advantage of this ultra-high gate-to-channel electric field found in smaller geometry CMOS integrated circuits by operating as a double-layer plasma instead of relying on semiconductor properties for conduction which are thermally, parametrically, and leakage current sensitive as all the channels operate in a strong-inversion mode. This way, CiFET™ parameters are only dependent on the relative ratios of the individual channel strengths which are set by the iRatio™ and cmRatio at physical layout. Strong inversion empowers high-speed and low noise from low resistance operation.

CiFET™ operation passes the same current through all channels while sharing the same ~midpoint common gate voltage bias $V_{cm}$ to define its output and input voltages. iPort™ injected current directly combines with this bias current to impose different current values in some of the channels in order to force changes at the common drain output voltage node.

# Analog FET baseline for CiFET™ operation

**MOS channel charge during sub-threshold (biased in weak inversion)**

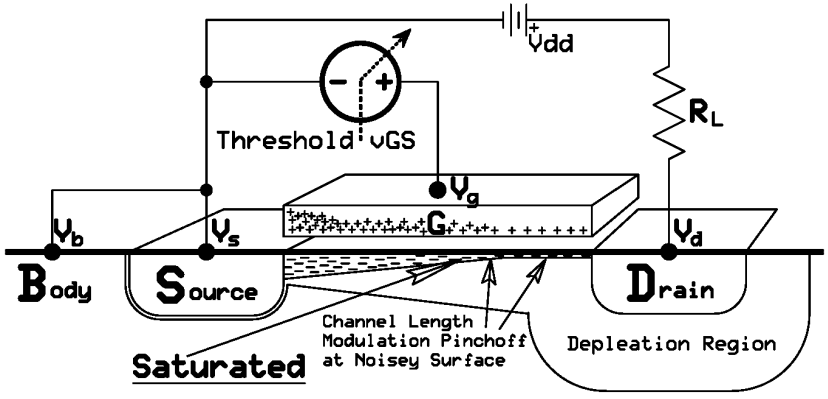
Weak inversion operation has high gain that is exponentially driven by channel diffusion having many decades of dynamic range, but is too weak and noisy from its high resistance and surface conduction. Channel conduction by diffusion results in exponential gain as opposed to the quadratic E-field driven conduction. It has been said that getting weak-inversion to go fast is the holly grail of electronics. The CiFET™ not only fills this void, but overshoots the target and with low noise and linearity.




Current driven by diffusion, very high impedance
Highest gain operation

**MOS channel charge during saturation (biased in strong inversion)**

Strongly saturated inversion operation has relatively low quadratic gain driven by the voltage gradient along the conduction channel having a few decades of dynamic range. Although the basic channel operates with lower resistance, analog applications require a high output resistance to achieve $g_m$*RL voltage gain demanding the pinch-off saturated mode of operation where noise and velocity saturation are prevalent.

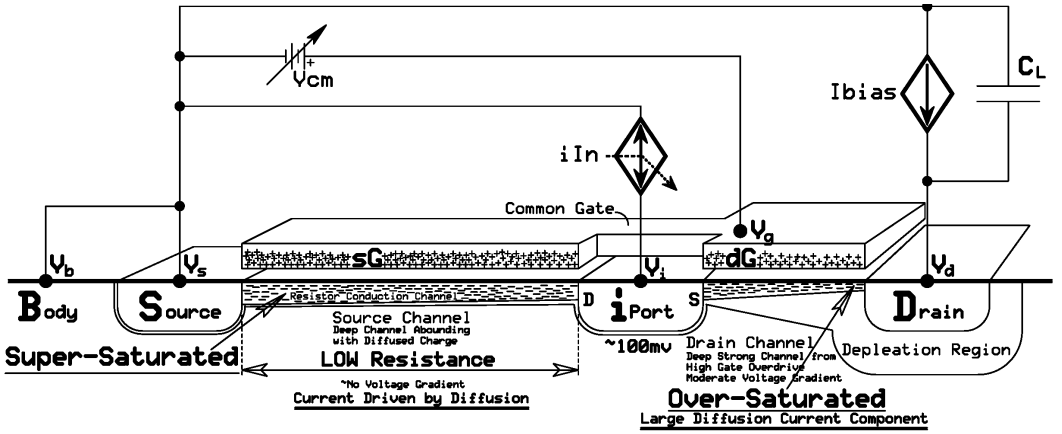



Current driven by voltage gradient, high impedance
Moderate gain operation

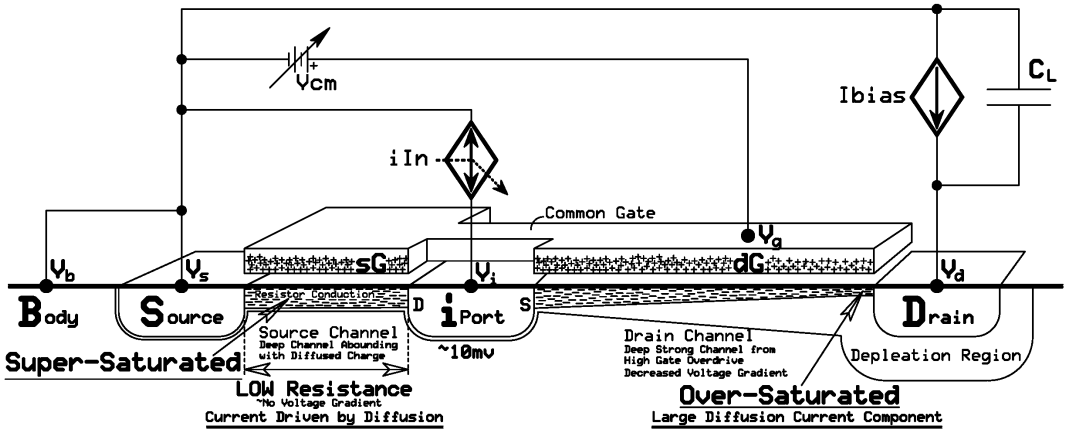
# 3-D half-CiFET™ iRatio™ channel charge distribution

Ratioing the relative half-CiFET™ channel sizes sets the CiFET™ design properties mostly independent of IC process parameters. The channel charge distributions provide insight to the exponentially driven diffusion currents and low operating resistances

**Vcm biased voltage-gain ($r_m$) mode**
**Half-CiFET (iRatio = ¼)**



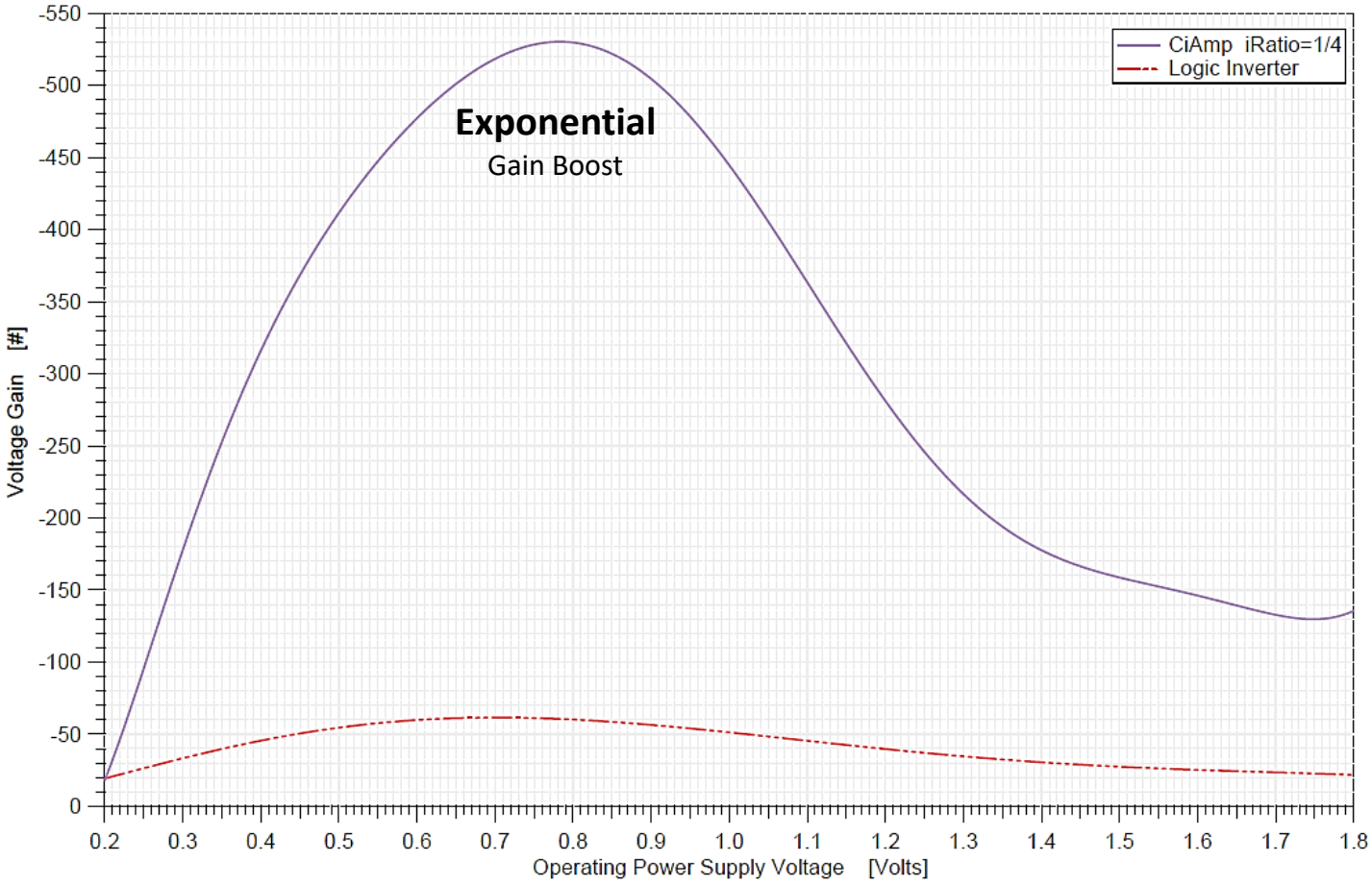

**Vcm biased input resistance ($R_{in}$) mode**
**Half-CiFET (iRatio = 4)**



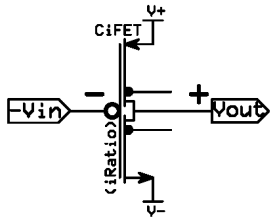
# CiFET™ Operation

**CiFET™ operation is exponentially boosted at nanoscale power supply voltages**
(similar to weak inversion, but very-fast and low-noise as a result low operating resistances)

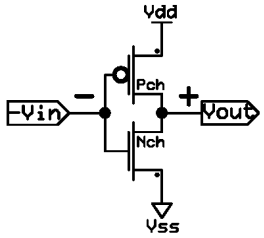
CiFET™ voltage-gain compared to a logic inverter voltage-gain using 180nm digital IC process



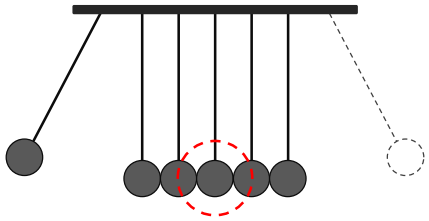

**CiAmp**




**Logic Inverter**



# Newton's cradle of collision as an analogy of CiFET™ super-saturated channel conduction



Newton's Cradle provides intuitive fingertip perception of CiFET™ strongly-inverted charge-mode channel operation as essentially exponential diffusion-driven/sub-surface conduction, as opposed to conventional E-field (square-law) driven surface conduction, thus yielding high exponential gain similar to weak inversion, but on steroids (high-speed with low impedance), from parasitically independent small low input resistance voltage changes while operating at noise levels comparable to sub-surface j-FETs.

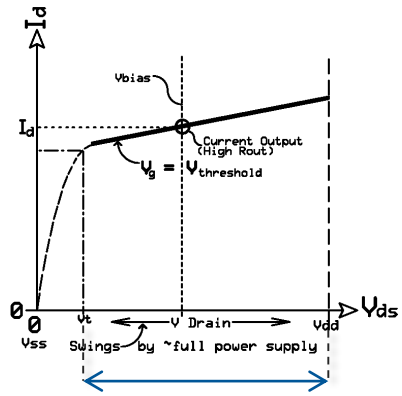
CiFET™ charge transmission, or current, is an extremely high-speed mechanism resulting from carriers passing their energy from one carrier to an adjacent carrier, instead of carriers traveling through the channel. Energy transferred through the balls resemble rapid charge movement, causing a much higher charge transfer velocity through the dense concentration of carriers, thus being nimble as compared to individual charge carriers passing through their channel. This conduction mechanism circumvents speed (frequency) limiting velocity saturation. Notice that the full signal source energy is absorbed into and used by the channel to instantaneously produce an output signal on the other end, circumventing carrier transient time, conduction collision, and surface conduction noise. Low channel resistance also contributes to low Johnson-Nyquist noise.

The right dotted ball represents charge entering the super-saturated channel's chain of balls in contact with one another. Energy entering the chain is slow in comparison to rapid energy transmission through the chain (where the balls do not move significantly) and rapidly progressing out the other end, where the last ball continues to carry the input energy.

In addition to limited charge movement, there are additional CiFET™ low noise benefits as most of the charge carriers are electrically distributed (like charges repel each other) away from the defect laden surface lattice traps under the gate. Also, contributing to lower noise, the strongly-inverted CiFET™ drain channel typically operates with its drain voltage equal to its gate voltage, thus eliminating the pinched region of a saturated MOS channel that is required in conventional analog $g_m*(R_{out}||R_L)$ gain applications for high output resistance.

# “Duality” operation of complementary FET channels used in the CiFET™

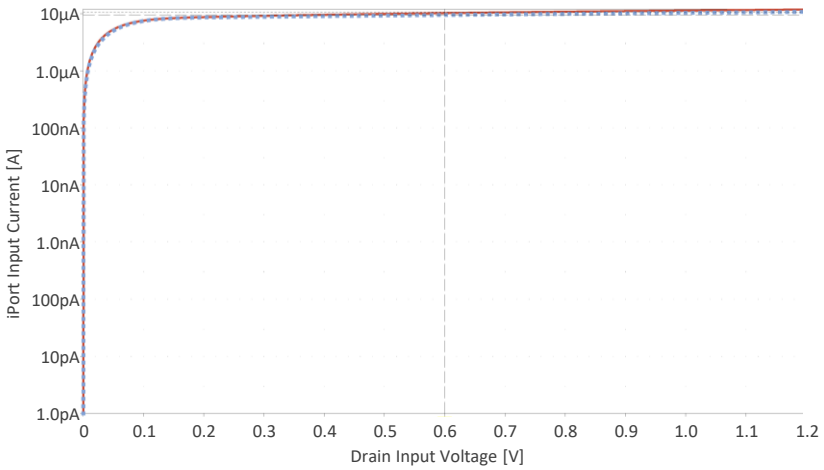
## Conventional FET



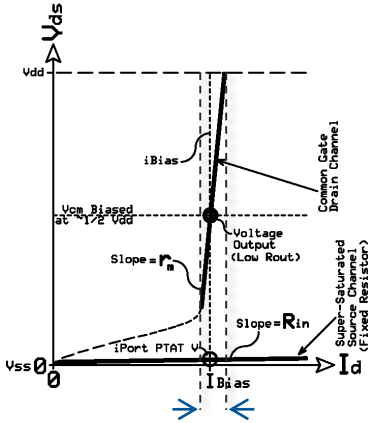

Large input dynamic range
yields a small output dynamic range

Overlay of conventional biased N-FET and P-FET transistors sized for similar strength.

Both input impedance and output impedance are ***high***, making them sensitive to loading and surrounding interference coupling.



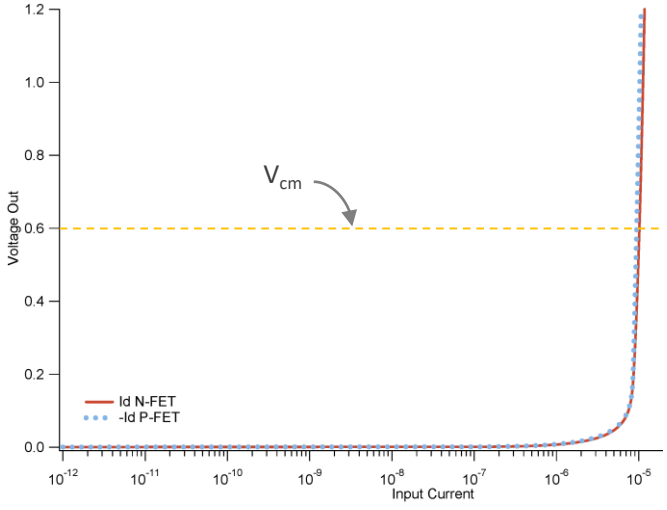

## CiFET™




Small input dynamic range
yields a large output dynamic range

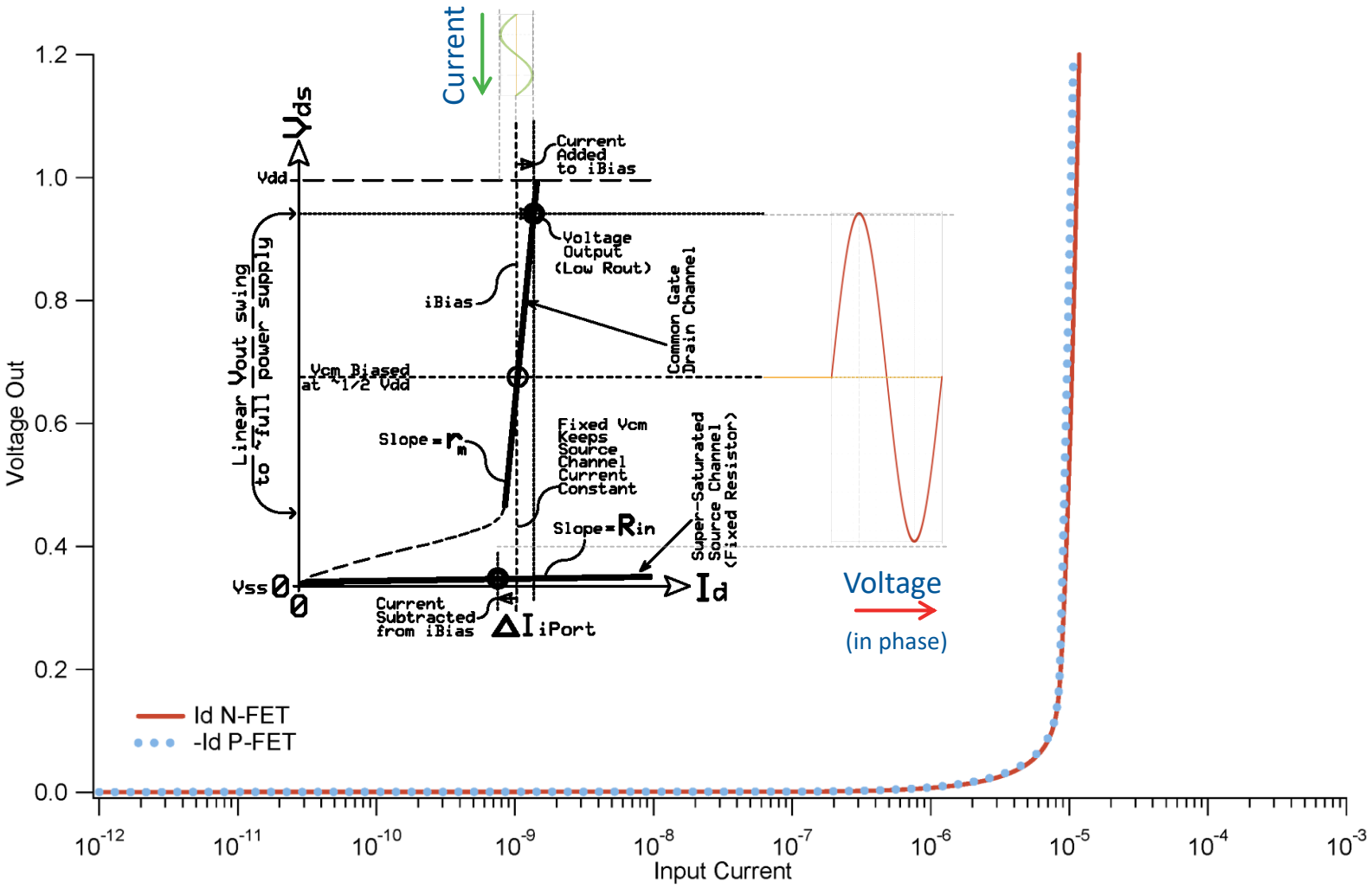
The CiFET™ flips the axis (duality) and uses iPort current as the input variable and drain voltage as the output variable.

Both input impedance and output impedance are ***low***, making them insensitive to loading and surrounding interference coupling.



# CiFET™ Channel Fusion Action

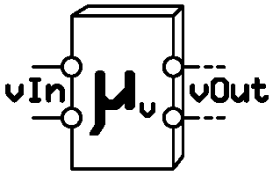
Fused interaction of CiFET™ channels convert small iPort current input to a relatively large & stiff voltage directly



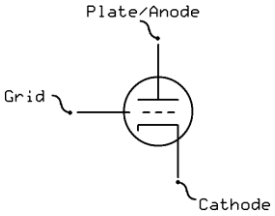
# All 4-Possible Amplifier Network Categories

Input and output variables of interest (either current or voltage) are ***state*** variables while other pair are ***incidental*** variables in that they "are what they are" in order to drive the state variables.
This consideration classifies the 4 possible network categories which amplifiers fit into.

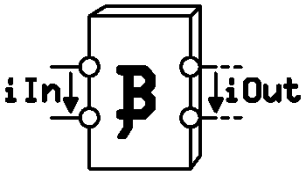
## Triode
Vacuum Tube



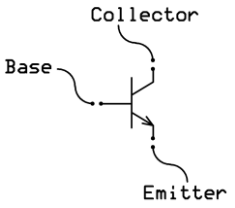

Voltage in → Voltage out
(mu $\mu_v$)
**Analog functionality**



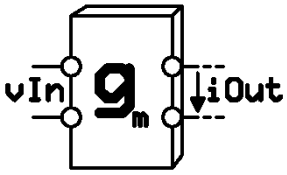

## BJT
Bipolar Junction Transistor



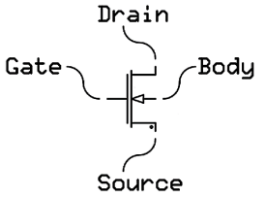

Current in → Current out
(Beta $\beta$)
**Analog functionality**



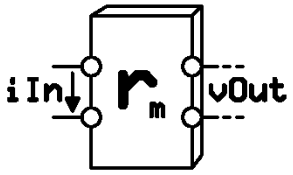

## FET
Field-Effect Transistor



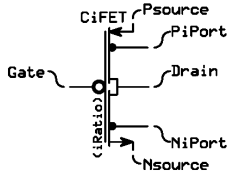

Voltage in → Current out
(Trans-Conductance $g_m$)
**Digital functionality**




## CiFET™
Complementary Current Injection Field-Effect Transistor

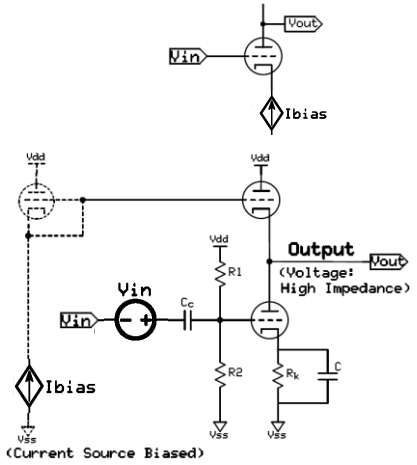



Current in → Voltage out
(Trans-Impedance $r_m$)
**Analog functionality**

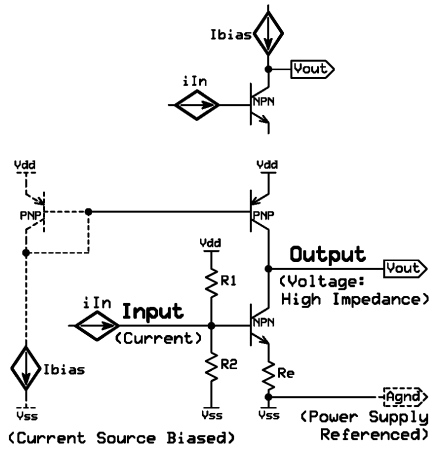


# Amplifier Categories

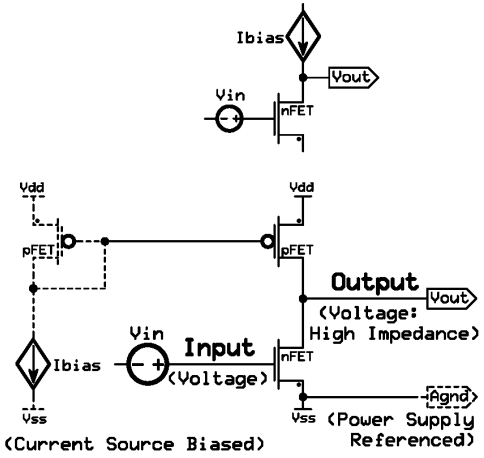
**Triode / Vacuum Tube**



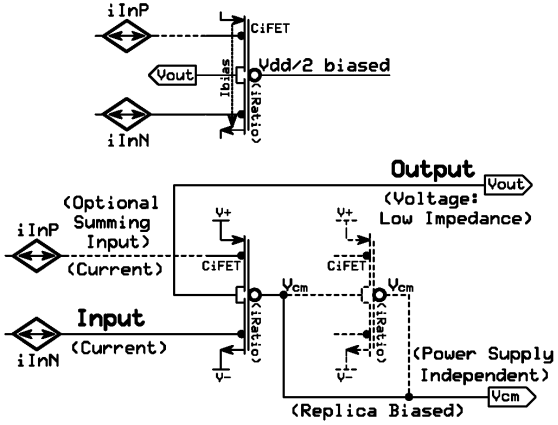

**BJT**




**FET**




**CiFET™**



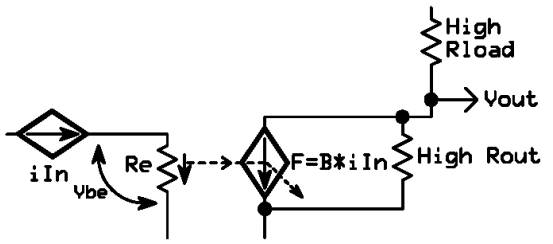

**CiFETs do not require current mirrors**

*Note: Current mirrors are not available in nanoscale*

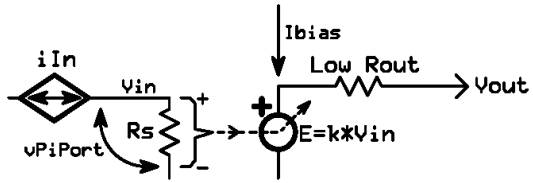
# Small-Signal Model

BJT & iFET have similar current inputs which are offset referenced to a supply

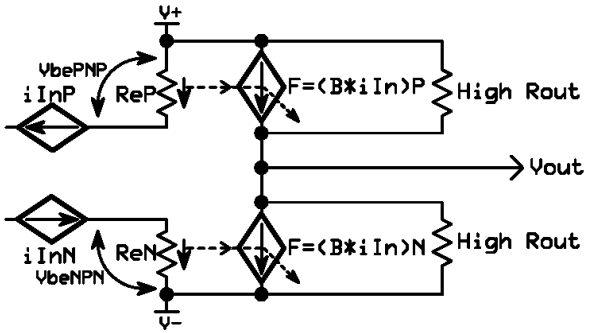
BJT



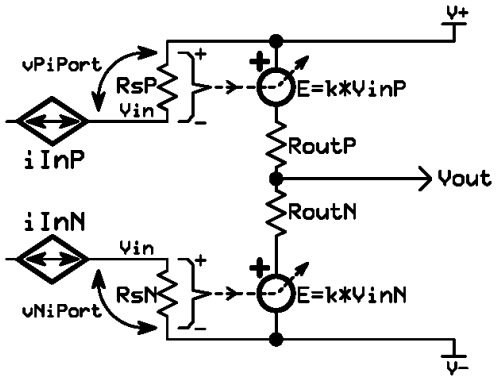

iFET




BJT Inverter



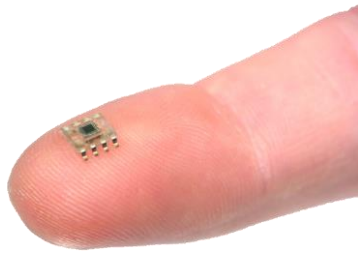

CiFET™




CiFET™ iPort current is bidirectional inc zero

# Comparison of a BiPolar Transistor Amplifier to a CiFET™ Amplifier

CiFET™ iPorts operate similar to BiPolar transistor Base terminals, where small signal currents change their output voltage around an analog common mode voltage ($V_{cm}$). CiFET™ iPorts input to Source supply terminal models like the BiPolar Base input to Emitter supply terminal:



| | |
|---|---|
| CiFET™ iPort input is a fixed-resistance ($R_{in}$) | terminated into a PTAT voltage ($V_{iPort}$) |
| BiPolar base input is a current-dependent resistance ($r_e$) | terminated into a PTAT voltage ($V_{be}$) |

In both devices, the input current is the controlling input state variable while relegating input voltage to an incidental state variable: "it is what it is" – similar to input voltage of a current mirror.

A more sophisticated bipolar class AB amplifier introduces active pull-up, but in doing so introduces crossover distortion which engages a nonlinear transfer function. The CiFET™ output is constrained to a linear I/O relationship by reason of loading its exponential pull-down iFET to a complementary exponential pull-up iFET, empowered by the N-iFET and P-iFET passing the same steady-state current through both devices while sharing gate voltage, thus canceling out their parametric discrepancies and non-linarites. A change in current does the same to all P-iFET and N-iFET channels, yielding a linearized output voltage due to the common totem-pole current/gate voltage combination. The complementary pull-up load logarithmically cancels the iPort exponential input behavior, which is essentially flawless over greater than 9 decades of dynamic range.

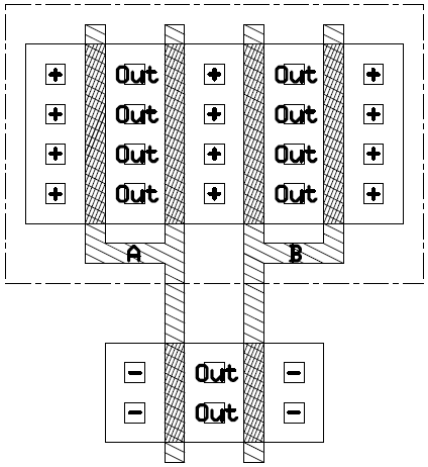
Instead of being dependent on widely varying semiconductor parameters, the iRatio primarily sets the operating properties at design/layout granting stable predictable high gain amplification with a virtually vanishing footprint with ultra-low power consumption. The CiFET™ circumvents the requirement of analog IC process extensions, yielding a scalable logic-only IC process compatible nanoscale amplifiers. Since the CiFET™ is a trans-impedance device, gain increases with process shrink (CiFETs™ thrive on low $R_{out}$) as opposed to trans-conductance MOS amplifiers requiring high $R_{out}$ which degrades intrinsic gain to 1 at about a 5nm IC process node. The simplicity and linearity of the CiFET™ offers straightforward clean analog circuit implementations with simple solutions to functional limitations.

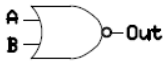
# CiFET™ Planar and FinFET Physical Layout Plans

CiFET™ layout plans for planar and FinFET technologies using iRatio of ¼ and 4 with a comparison to a 2-Input NOR Logic gate. Inverting the iRatio only requires reversing the CiFET™ metal connections to make current pass in the opposite direction through the iFET transistors.

## NOR Gate

cmRatio=2

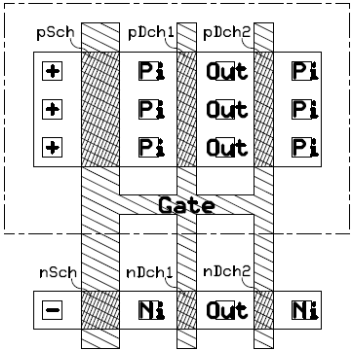


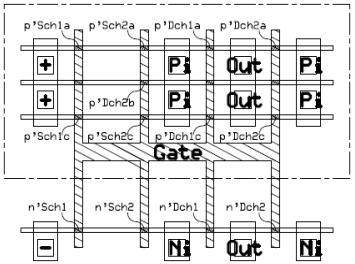



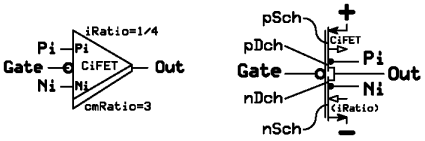

*The CiFET™ is about ½ the area of a small NOR-2 logic gate*

## Voltage Mode Applications

$r_m$ iRatio=¼, cmRatio=3

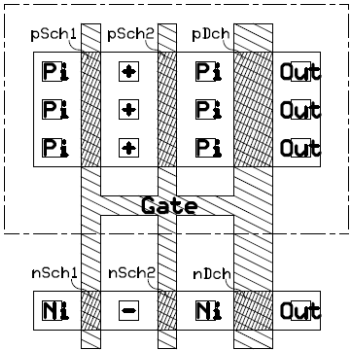


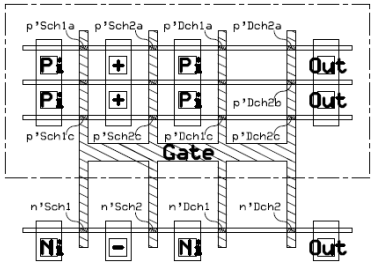



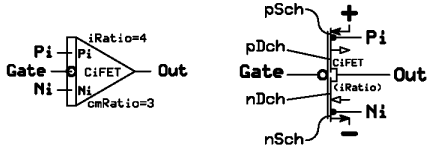




## Current Mode Applications

$R_{in}$ iRatio=4, cmRatio=3



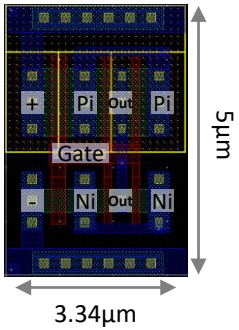



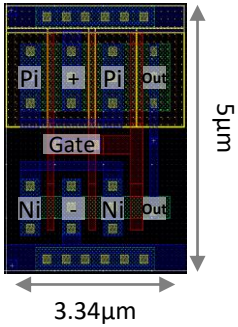
# CiFET™ Physical Layout

IBM/Global Foundries 130nm IC Process

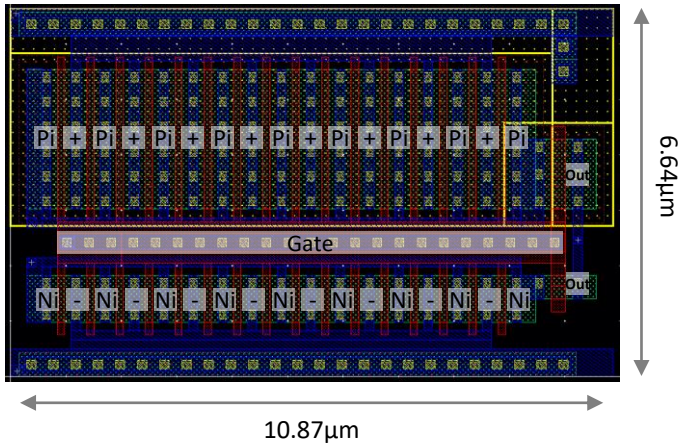
iRatio = ¼




iRatio = 4




iRatio = 64




The higher trans-Impedance gain $r_m$ CiFET™ iRatio™ of ¼ is employed for it's cascode voltage gain properties in the 3-stage CiAmplifier™ types of applications. Additional low impedance inputs at either iPort™ have an input resistance of about 35KΩ, that can terminate a filter network. For example, in a multi-stage CiFET™ amplifier, the first stage iPorts™ are used for roll-off.

The lower $R_{in}$ CiFET™ with a ratio of 4 is obtained by simply interchanging the ¼ ratio $r_m$ CiFET™ internal power/output connections. Shown here with the output on the extreme right (vertical blue metal wire) instead of one transistor in from the right. This configuration has about 1 KΩ input resistance at the iPort™ which can be set by the CiFET™ ratio for transferring sensor energy directly into the CiFET™ channels where it participates in the transfer of input charge to voltage output.

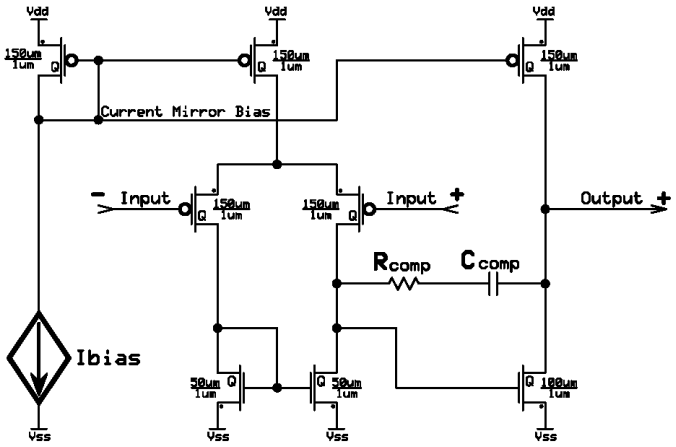
The CiFET™ ratio of 64 has about a 100Ω iPort™ input resistance which is used to terminate a 100Ω transmission line or antenna while applying input energy into the operation of the CiFET™ voltage output.

# CiFET™ Voltage Amplifiers

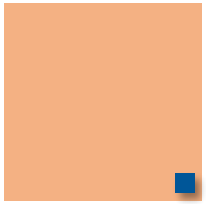
High voltage gain ultra-linear CiFET™ core circuits with
high input resistance and low output resistance

# Operational Amplifier Intrinsic Core

## Conventional CMOS OpAmp [6]

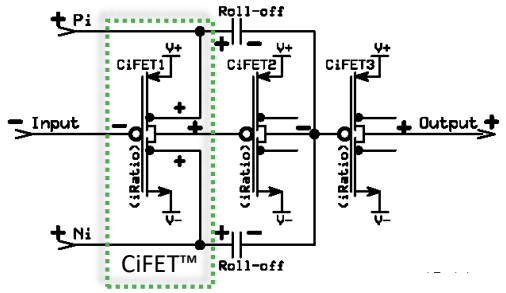



- 8+ Large (for linear gain) CMOS transistors;
- High output impedance for $g_m * R_L$ gain;
- 1 medium tolerance resistor (100Ω - 1kΩ);
- 1 large capacitor (~5 to 10pf);
- Consumes a large chip area;
- Slow overdrive recovery;
- Stability sensitive to capacitive loading;
- Requires tight Vdd around 1.8V or higher;
- Power hungry current bias and mirrors;
- Not easily portable (requires redesign);
- Not scalable to smaller process nodes.



Surface Area

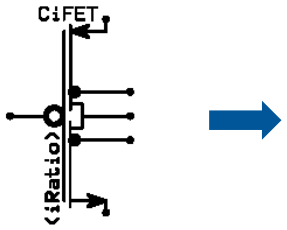
## 3-Stage CiAmp™



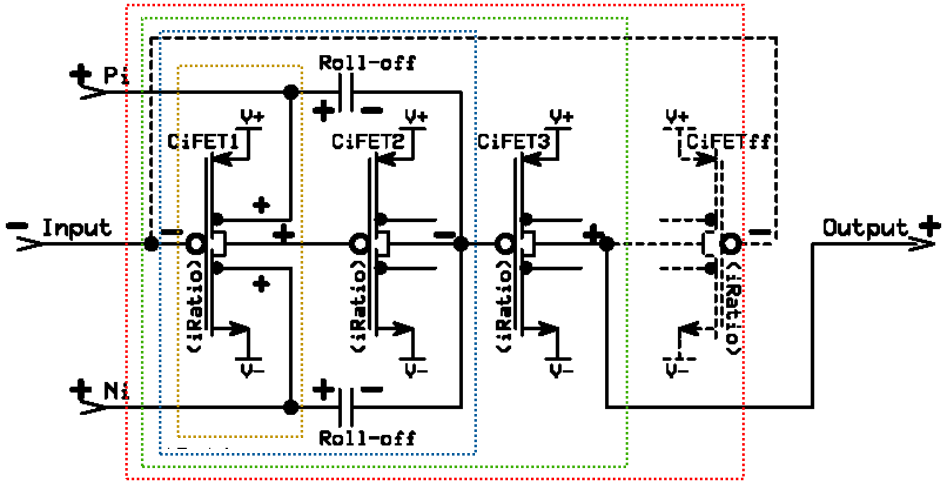

- ✓ 3 Minimum-sized CiFET™ transistors (6 CiFET™ for full differential version);
- ✓ No current mirrors;
- ✓ Self-biasing in circuit applications;
- ✓ 2 Small roll-off capacitors (~50 ff);
- ✓ Unity-gain stable over wide frequency range;
- ✓ Immediate overdrive recovery;
- ✓ High gain with high linearity;
- ✓ Crossover distortion free;
- ✓ Symmetrical Output drive;
- ✓ Low output impedance;
- ✓ Insensitive to capacitive loading;
- ✓ Wide supply voltages (200mV to 1.8V);
- ✓ Low power consumption;
- ✓ Portable / scalable to newest processes.

# CiFET™ Voltage Amplifier

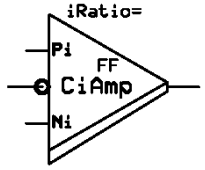
The higher trans-Impedance $r_m$ CiFET™ iRatio of ¼ is employed for it's cascode voltage gain properties in a 3-stage CiAmplifier™. Additional low impedance inputs at either iPort™ have an input resistance of about 35KΩ and are useful for terminating a filter network, bandpass shaping, and other current inputs. For example, in this multi-stage CiFET™ amplifier, the first stage iPorts™ are used for roll-off. This iPort™ application has the advantage of tracking IC process gain variation as a CiFET™ tracking Miller capacitance multiplier invoking the second stage a dominant frequency roll-off pole. This makes the second stage much slower than the sum of the other stages having a typical delay of about 4ns at a 130nm process node. The roll-off capacitance is symmetrically split between both of the first stage iPorts™ to balance noise and dynamic circuit operation. In high-gain multi-stage CiAmplifiers™, unity-gain compensation requires about 50ff roll-off capacitors.




Seminal CiFET™ as a component of the CiAmp™




3-Stage Feed– Forward CiAmp™




CiAmp™ symbol

**1-Stage**
Seminal CiFET™

**2-Stage**
Gain increase with roll-off compensation

**3-Stage**
Basic high gain configuration

**3-Stage Feed-Forward**
Increase speed at some cost in gain

# CiFET™ Voltage Amplifier

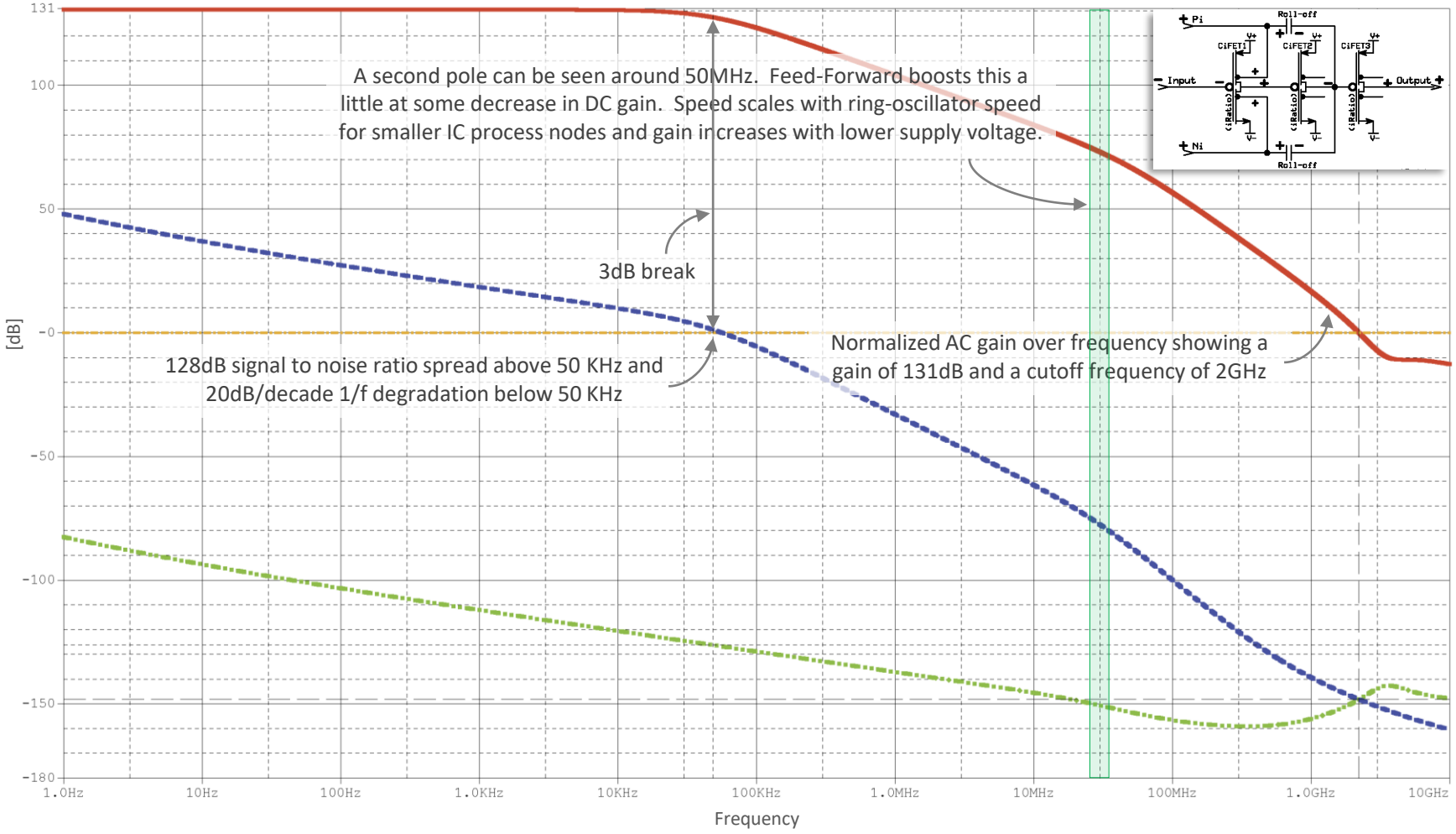
All CiFETs™ use the same CmRatio and CiRatio™. In operation, CiFET™1 voltage input terminal is systematically biased to its optimum common mode ($V_{cm}$) operating point, nicknamed "sweet-spot," found by temporally connecting amplifier input to output and storing this voltage on a capacitor. When operated about this self-biased voltage ($V_{cm}$), peak gain and dynamic range are captured independent of semiconductor parameters. Since all CiFETs™ share the same CmRatio and iRatio™, they also operate about this same "sweet-spot" bias voltage. Here the combined voltage gain is third-power of the individual CiFET™ gain. For example, a CiFET™ iRatio™ of ¼ at Vdd=800mV has voltage gain is 520 making CiAmp™ gain 140 Million or 160dB. When the output signal swing is large, the gain of CiFET™3 moderately diminishes, but the combined gain remains high because the preceding CiFET™ stages still operate at their maximum "sweet-spot" gain. The smaller the IC process node, the less CiFET™3 gain depends on output voltage level operating near $V_{cm}$. Paralleling 2 or more identical CiFETs™ to CiFET™3 increases output drive. A parallel CiFET™1 decreases input noise while boosting gain a little.

When the CiAmp™ operates at unity-gain, the 3-stage CiAmp™ becomes a ring oscillator. Making CiFET™2 much slower than the sum of the other CiFET™ delays, establishes stability by making the 3-stage amplifier appear as a single CiFET™. Augmenting CiFET™2 Miller capacitance with a token capacitance (~100ff for a 130nm process) and amplifying the augmented Miller effect with the CiFET™1 trans-Impedance gain achieves unconditional stability that is slaved to IC process parametric variation. Splitting these roll-off capacitors between the two existing CiFET™1 P&N-iPorts provide additional symmetry. Feed-forward performance is achieved by a wire-OR of an additional inverter around the multi-stage inverting amplifier to speed-boost (up to an order of magnitude) the initial propagation delay of the single feed-forward inverter. A single inverter is always closed-loop stable. After the initial push, the output is trimmed-in by the high-gain path at the slower time of the full CiFET™ chain. Wire-OR works because both forward paths are going to the same output voltage.

To increase gain for IC processes and applications that have inadequate CiFET™ gain, series pairs of CiFETs™ can be chained to make a 5- or 7-stage CiAmp.™

# Open Loop Gain and Noise Over Frequency

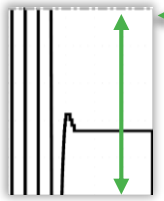
AC Frequency response of a minimum area CiAmp™ without feed-forward in 180nm operating with a 1.8 volt supply



# 3-Stage Feed-Forward CiAmp™ Time Domain Response Plot

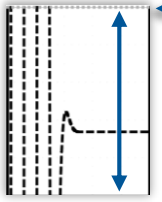
Input and output signal perturbation 1,000,000x magnified to 1µV scale (1PPM resolution = 20 bit accuracy in linearity and gain)

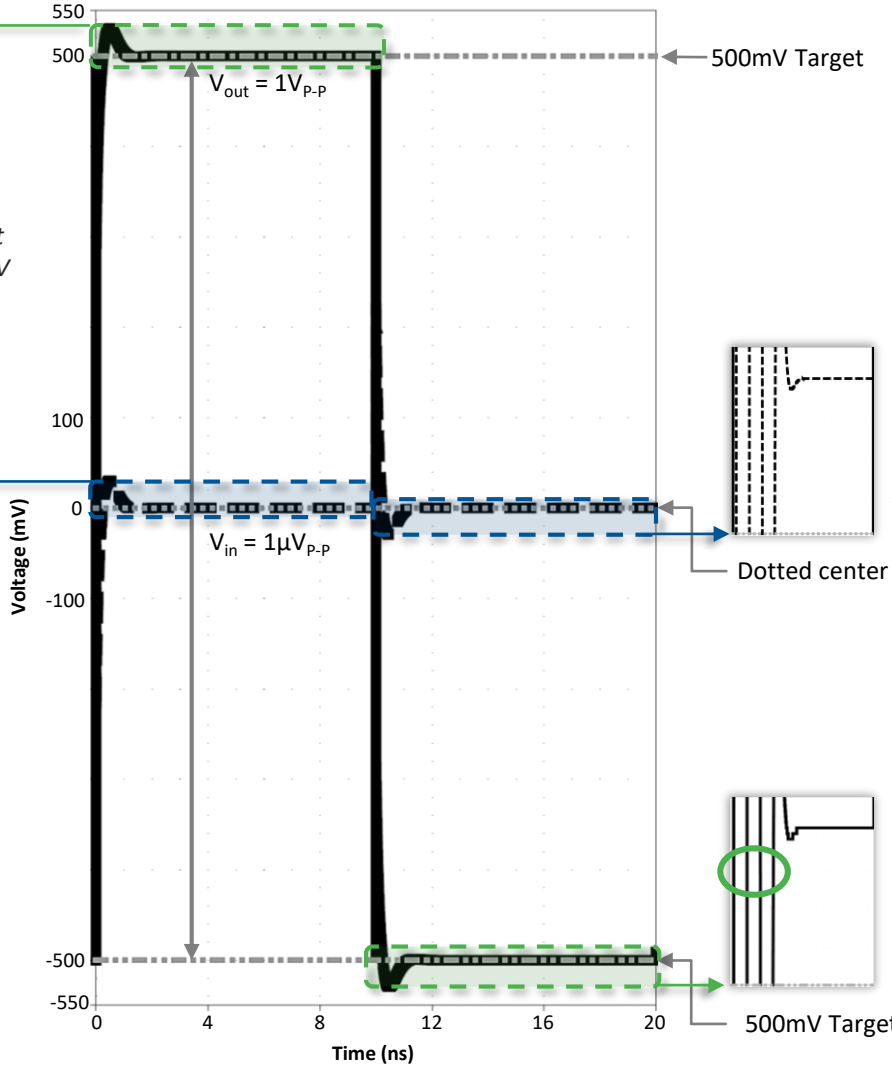
**+ Output Signal Perturbation**
*Exponentially decayed ringout resulting from 3% underdamped overshoot*



*2nd order system overshoot is set to 3% of target = 30mV (Inserts are ½ cycle wide)*

**+ Input Signal Perturbation**
*The positive pulse reaches **+500mV** target within **0.6µV** via pushing the input down by 0.6µV*






**- Input Signal Perturbation**
*The positive pulse reaches **-500mV** target within **0.8µV** via pushing the input down by 0.8µV*



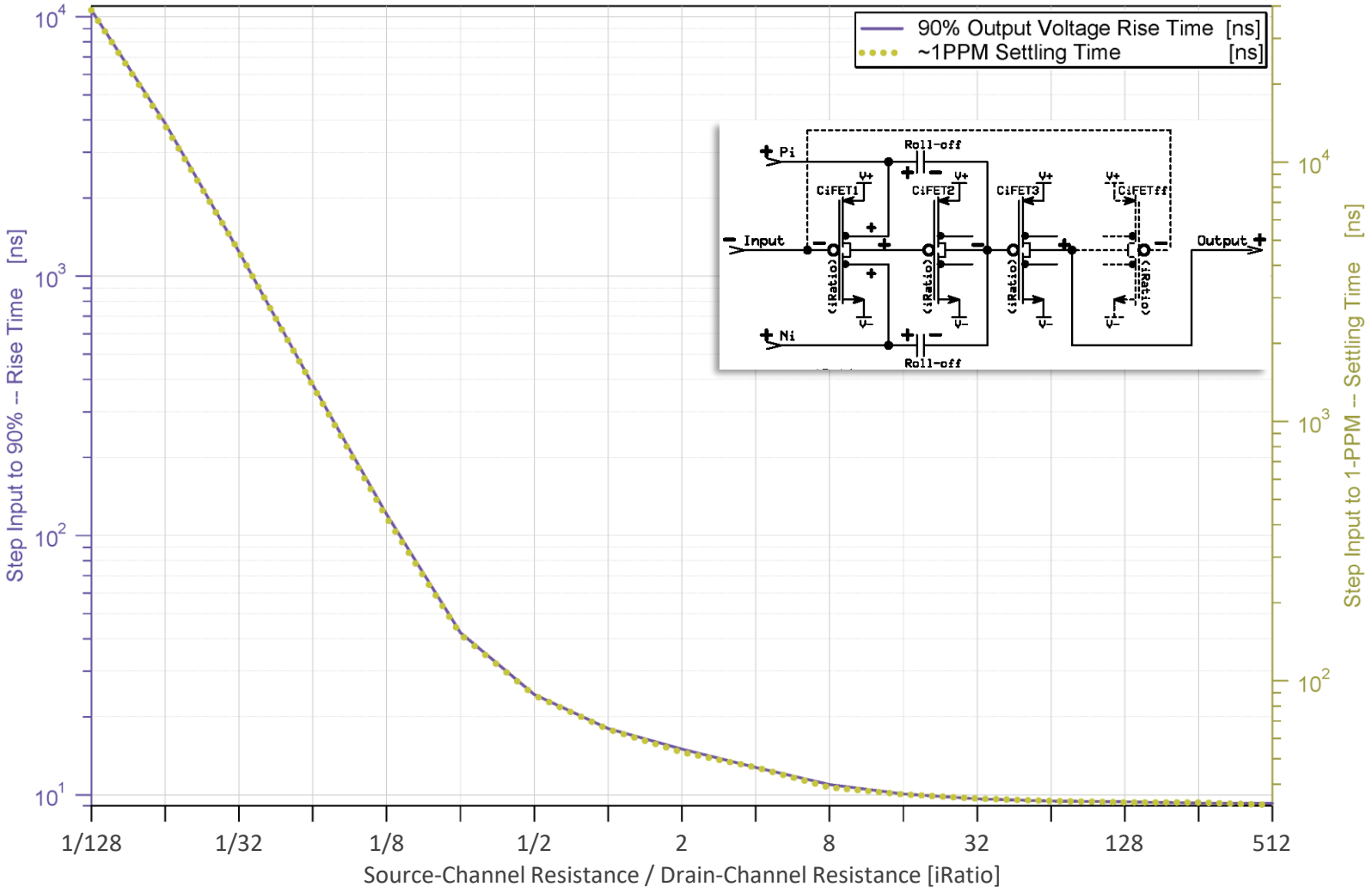
**- Output Signal Perturbation**
Highly magnified ring-out as the feed-forward inverter gets there first while triple CiFET™ gain fine-trims the output to PPM precision.



Key:
- Amplifier Input
- Amplifier Output
- Upper Target
- Zero Reference
- Lower Target

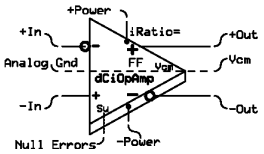
# 3-Stage Feed-Forward CiAmp™ Settling Time

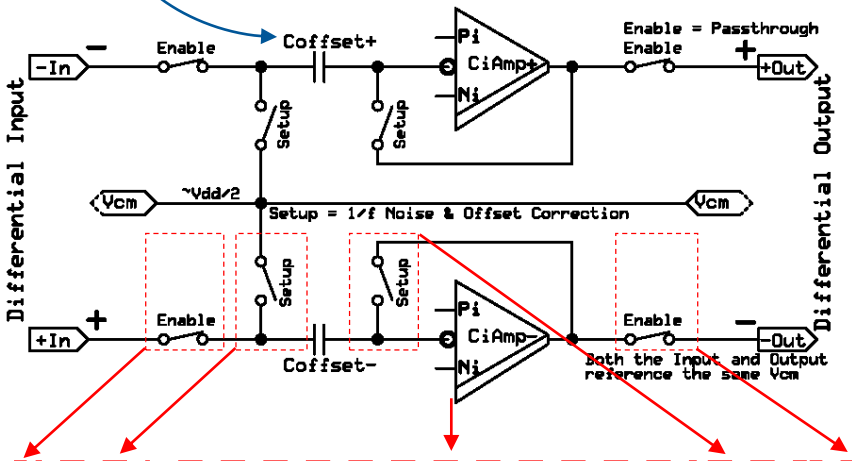
Speed in terms of 90% Rise-Time ($t_r$) or 1-PPM (20-bit resolution)
Settling-Time ($t_s$) vs iRatio™) for a 180nm Logic IC process node

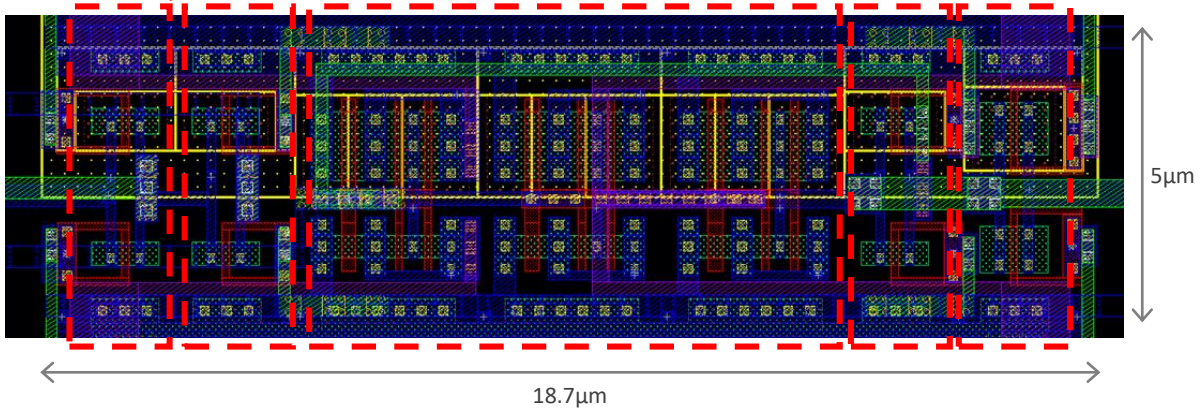


# Differential Input – Differential Output CiOpAmp™

Coffset capacitors translate from $V_{cm}$ to the optimal CiFET™ operating bias voltage

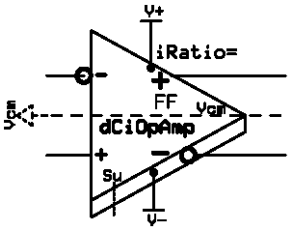


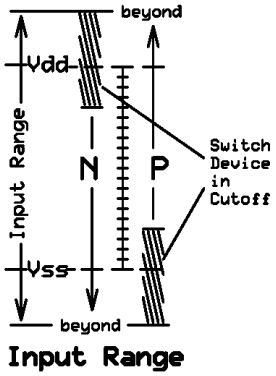



# Differential Input – Differential Output CiOpAmp™

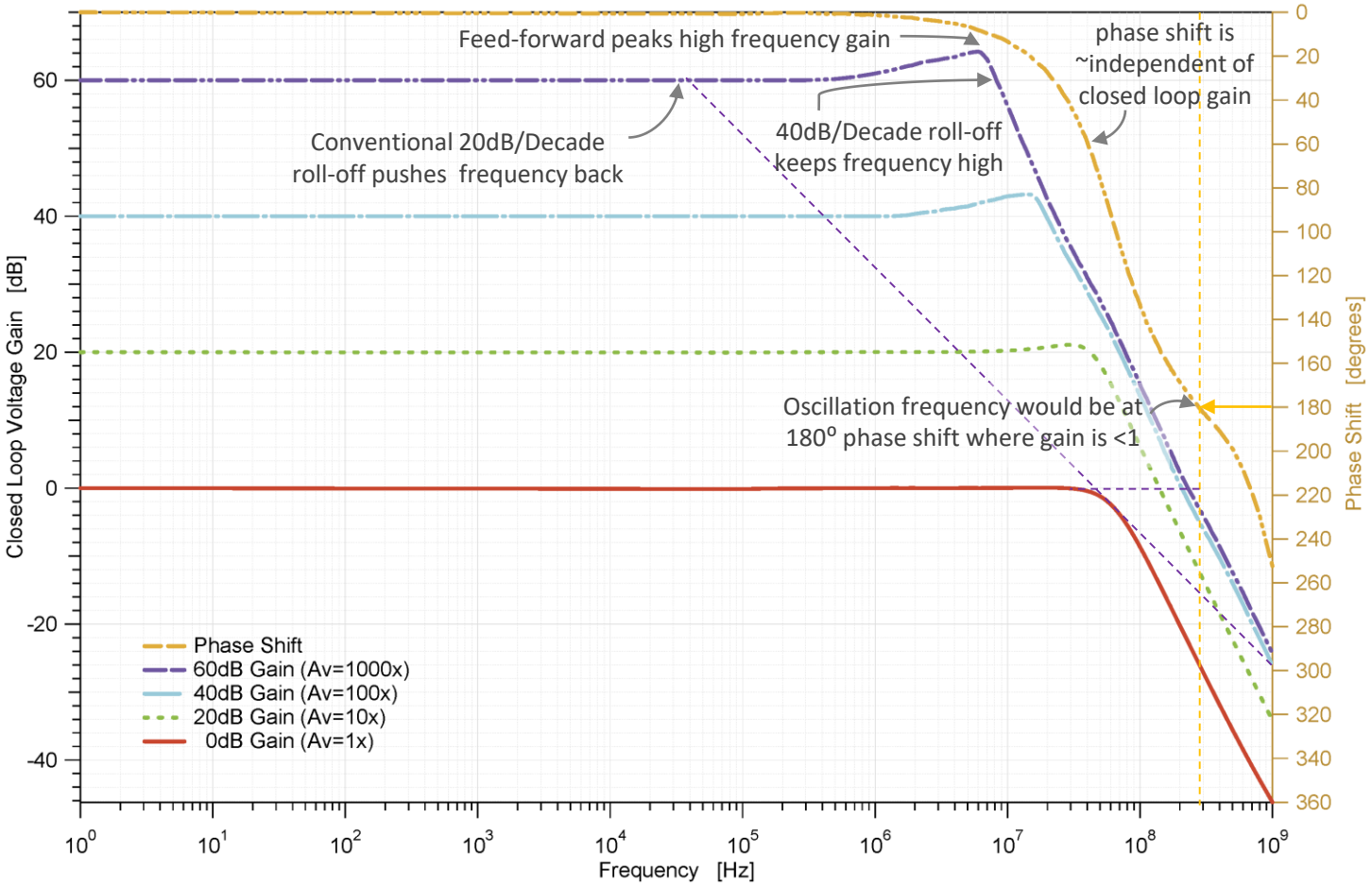
- Due to the differential properties, the CiOpAmp™ output can effectively swing twice the power supply voltage. This especially beneficial for the <1 volt supplies required for the newer nanoscale IC process nodes
- Input dynamic range extends to a diode outside of both power supply rails. This is useful for sensing input signals that swing about a power supply rail or larger signals that exceed the rails
- Optimal at nanoscale process nodes
- Due to the complementary configuration, CiOpAmp™ offset voltage only needs to be corrected about once a second to maintain a ~1µV offset accuracy. This low offset correction rate is a consequence of differential leakage and differential offset drift cancelation. For nullifying 1/f noise this sampling rate is optimum around a ~1ms calibration rate where offset can be corrected to about 10nV
- The CiOpAmp™ "Enable" switches disconnect the CiAmps™ from its source and load during a brief calibration period, leaving the output load capacitance holding the output momentarily. During this ~1µs calibration time, the CiOpAmp™ input and output is disconnected and looped back around the CiAmp™ cores for sampling its instantaneous offset and noise voltage
- Minimum operating $V_{dd}$ is limited by switch turn-on voltage



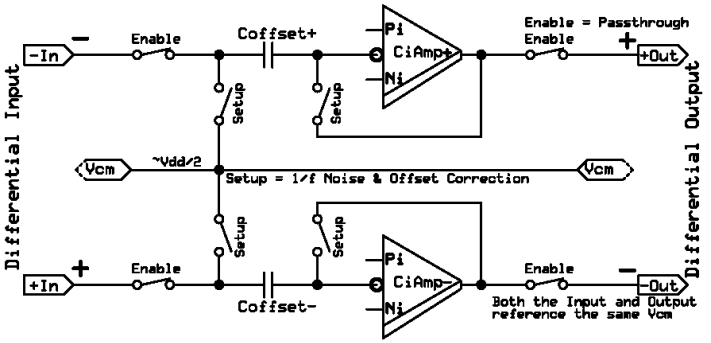
# Closed-Loop Gain, Frequency, and Phase Response

The full-differential CiOpAmp™ maintains a persistent wide bandwidth with a ~fixed phase-shift as closed-loop gain is increased. This is a result of the constant delay CiFET™ augmented Miller capacitance roll-off approach, which pushes out high-frequency closed-loop gain using a 40dB roll-off slope. Roll-off is enacted from constant delay of the second stage CiFET™ to form a ~ constant bandwidth amplifier ~independent of its closed loop gain feedback circuitry providing an always stable amplifier, even at unity-gain. The incorporation of the feed-forward option peaks the high-frequency gain to get to target output voltage faster when necessary.



# Offset and Gain is insensitive to On-Chip-Variation (OCV)

Yield and reliability limiting Issues of single point parametric deviations (On-Chip-Variation - OCV) of ~40% have been observed in nanoscale IC processes.[1] This table lists the worst 5% deviation sensitivity tests and 50% OCV tests where individual channel widths have been increased to shake out sensitive devices in the Full-Differential CiFET™ OpAmp. The most sensitive point is the Offset Switch which has about a 35µV offset for a 50% change.

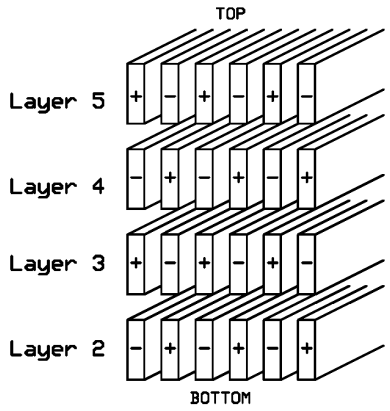



| Imposing individual 5% single channel strength errors (Normal parametric limit) | | | | | | | Imposing individual 50% single channel strength errors (Over-the-top parametric deviation) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| All Units are in µV | | | | | | | | | | | | |
| Channel | Output Peak | Output Valley | Input Refereed Offset | Output Amplitude | Gain Error | Description | Channel | Output Peak | Output Valley | Input Referred Offset | Output Amplitude | Gain Error |
| None | 100.050 | -99.985 | 0.006 | 200.035 | 0.035 | | None | 100.050 | -99.985 | 0.006 | 200.035 | 0.035 |
| Nss+ | 117.475 | -82.563 | 3.4912 | 200.038 | 0.038 | Offset Switch | Nss+ | 275.098 | 74.976 | 35.007 | 200.123 | 0.123 |
| Nss- | 82.559 | -117.494 | -3.4935 | 200.053 | 0.053 | | Nss- | -74.968 | -275.010 | -34.998 | 200.043 | 0.043 |
| Pss+ | 82.661 | -117.379 | -3.4718 | 200.041 | 0.041 | | Pss+ | -73.574 | -273.661 | -34.724 | 200.087 | 0.087 |
| Pss- | 117.431 | -82.617 | 3.4814 | 200.048 | 0.048 | | Pss- | 273.713 | 73.660 | 34.737 | 200.053 | 0.053 |
| Nsu+ | 99.850 | -100.293 | -0.044 | 200.142 | 0.142 | Reference Switch | Nsu+ | 97.853 | -102.216 | -0.436 | 200.069 | 0.069 |
| Nsu- | 100.318 | -99.792 | 0.053 | 200.110 | 0.110 | | Nsu- | 102.205 | -97.785 | 0.442 | 199.989 | -0.011 |
| Psu+ | 100.253 | -99.841 | 0.041 | 200.094 | 0.094 | | Psu+ | 102.194 | -97.868 | 0.433 | 200.062 | 0.062 |
| Psu- | 99.762 | -100.260 | -0.050 | 200.022 | 0.022 | | Psu- | 97.780 | -102.300 | -0.452 | 200.080 | 0.080 |

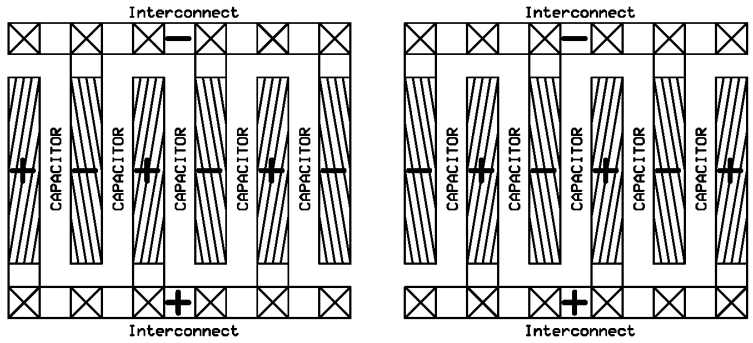
# MIM capacitors available in any IC

Construction of a Flying Fringe (Cordwood) Capacitor
using logic interconnect only

**Section View**
(Cut Away)

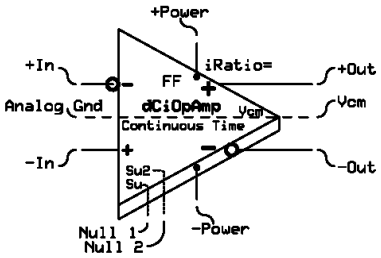


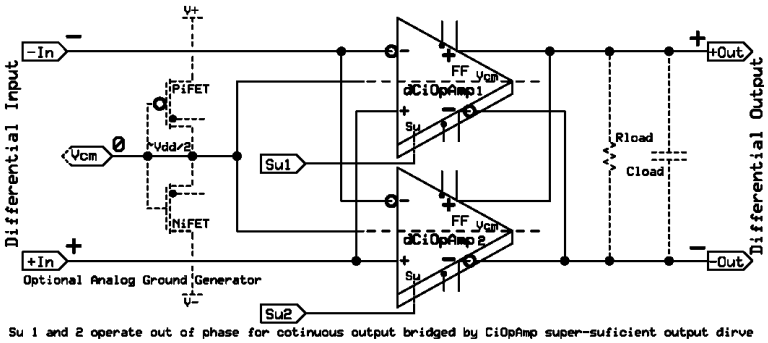

**Top View**
(Looking Down from Top View)




**M**etal-**I**nsulator-**M**etal flying capacitors are constructed from interconnect metal and existing insulation between metal traces. These are relatively low capacitance high-quality flying capacitors without voltage dependence and do not use substrate diodes, gate oxide, or analog IC process extensions. CiFET™ circuit capacitors are normally small enough to be size compatible with their active areas -- 50ff for roll-off and 700ff for offset correction are typical in 130nm. Smaller IC process nodes use proportionally smaller capacitances. The highest value precision CiFET™ circuit capacitors are normally limited to about 10pf. CiFET™ circuits generally do not use matched or precision capacitor values. Even number of constituent wires on the bottom layer and periphery tend to balance out external coupling into the stored capacitor charge. These capacitors can vary in structural use of contacts with consideration of sidewall fringe capacitance forming varying layout organizations which optimize them. Physical layout must conform with antenna rules as they are grounded through the transmission gate switches during manufacturing process. Nanoscale interconnect metal aspect ratio is thicker than wide as sketched, which is a consideration in cordwood construction.

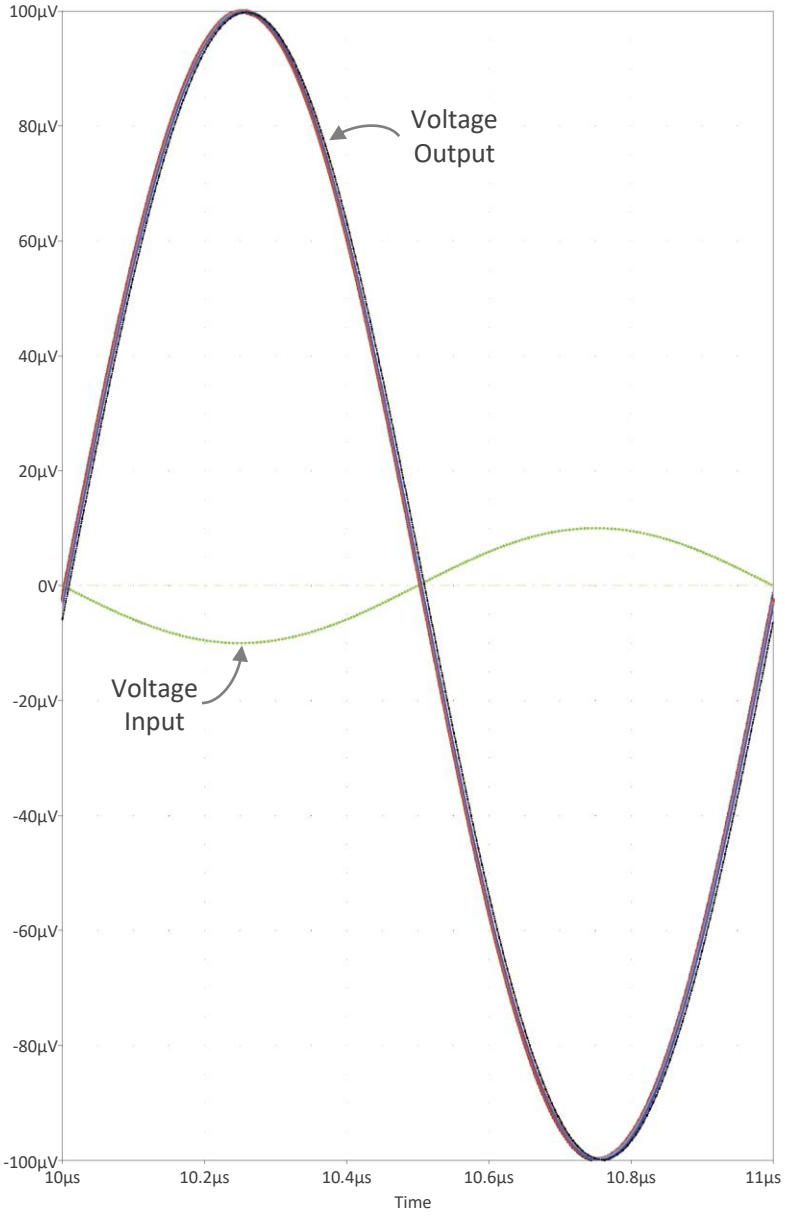
# CiOpAmp™ Derivative Example



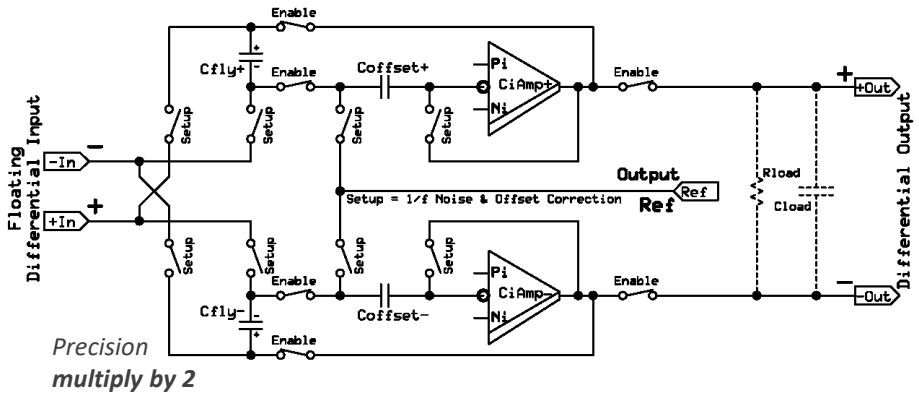



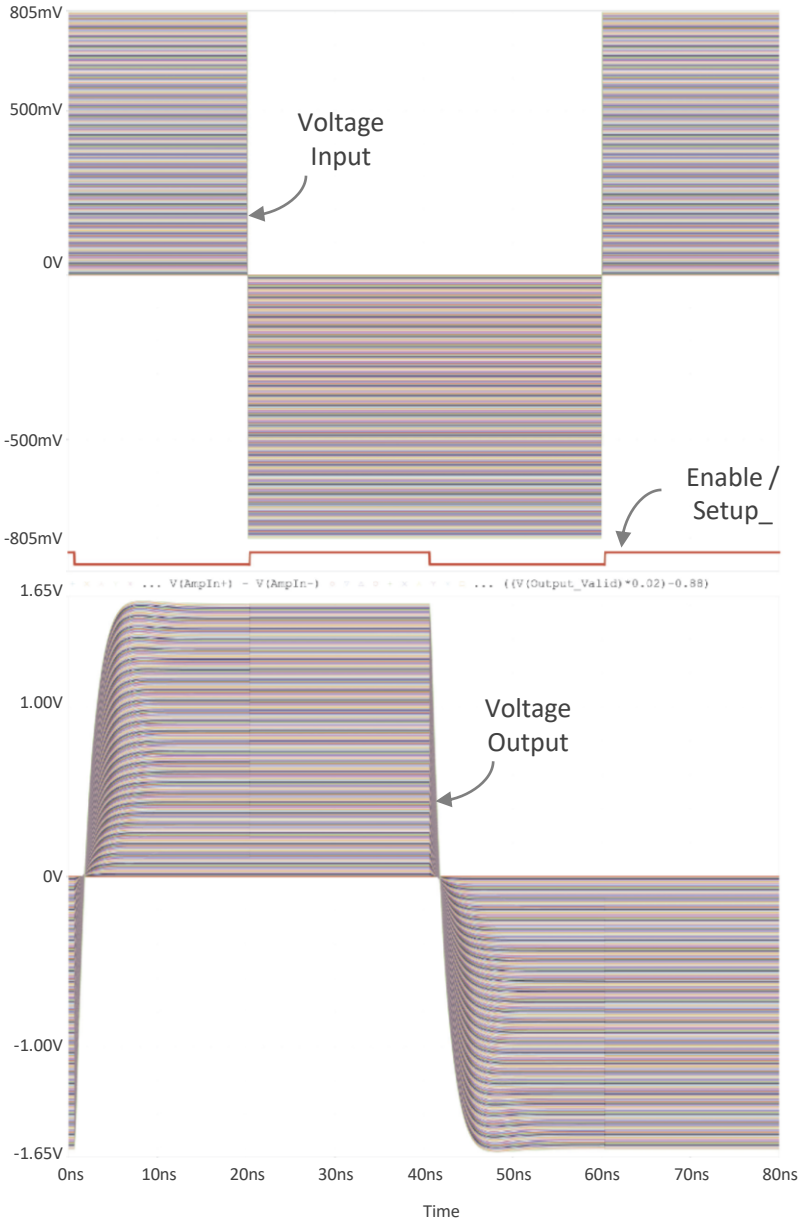

A **continuous-time CiOpAmp™** is formed by a wire-OR of two or more CiOpAmps™ which are dynamically calibrated out of phase from each other. Low output resistance maintains continuity while the other CiOpAmp™ is taken off-line for a typical ~1µs offset & noise cancellation cycle every ~millisecond. Reasonable offset can be held for over a second, but 1/f noise considerations argue for a one millisecond cycle time. Calibration time can be randomized.

The example waveform is included to illustrate that the CiOpAmp™ operates consistently over ±100°C wider temperature range than the full military temperature specification. A -10µv sinewave input to 100µv output is re-plotted over temperature from -150°C to +225°C in 25°C increments.



# Precision 2x multiplying CiOpAmp™ Derivative Example



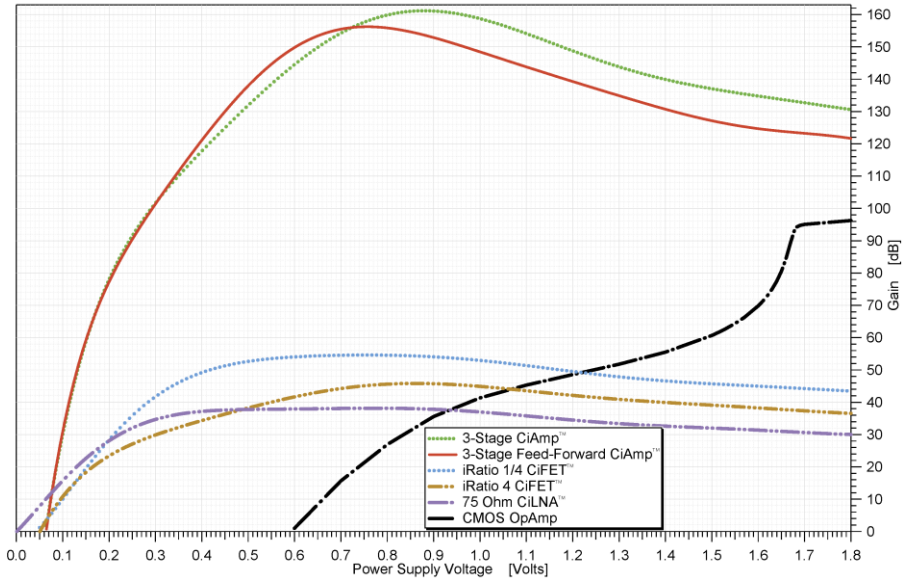




**Precision analog Integer multipliers** are constructed by charging capacitors during the "Setup" phase and then rearranging them during the "Enable" phase. The upper waveform is input voltage stepped with 350 progressive ±5mv increments, middle waveform is enable/setup_ clock, and the lower waveform is the 2x output voltage which is accurate to about ~1PPM (20-bit equivalent). Similarly, charging 2 pairs of capacitors in parallel and then putting them in series would precisely multiply by 4. Switching feed-through cancellation, bottom-plate sampling techniques, while maintaining a high series impedance after charging these capacitors preserves their charge and thus sampled voltage, rendering these capacitors equivalent to a battery during the enable phase of operation, resulting in a PPM level of precision being obtained without any tolerance restraints or matching requirements.

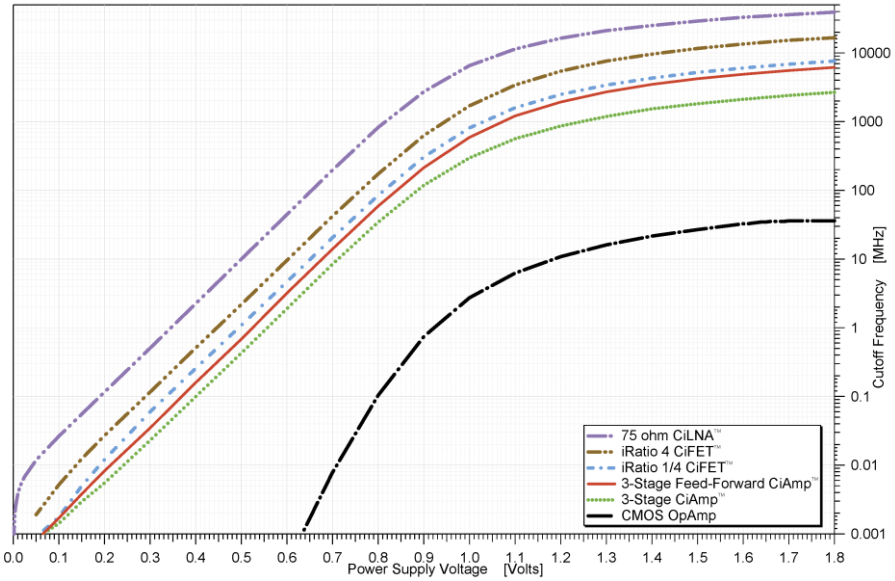
# Amplifier Comparisons

If high sensitivity, low noise at multi-GHz operating frequencies is sought after, the CiTIA™ (Complementary Current-Input Trans-Impedance Amplifier) is a notable example of the capabilities of the CiFET™ family of circuits

Voltage Gain [dB] vs. Supply Voltage [V]




Cutoff Frequency [MHz] vs. Supply Voltage [V]




**CiAmps™ have high gain without large analog transistors:**

- Voltage gain up to 160dB (100 million) whereas conventional CMOS prior art amplifiers [2] peak at ~100 dB (100k),
- As power supply voltage decreases (to ~500mV), gain peaks,
- Designs are compact due to minimally sized components,
- No analog IC process extensions required,
- Works in any complementary Field Effect Transistor process,
- Thrives in nanoscale Logic-only process nodes.

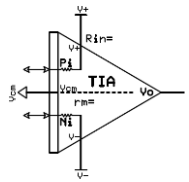
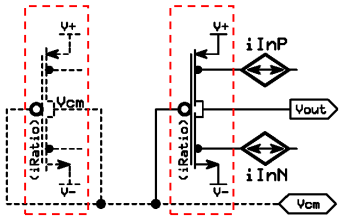
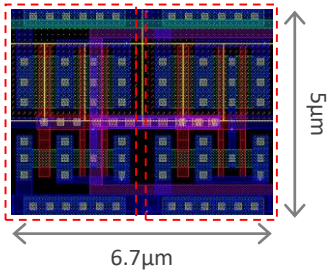
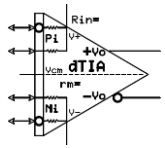
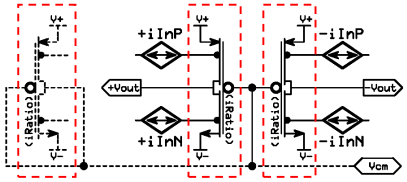
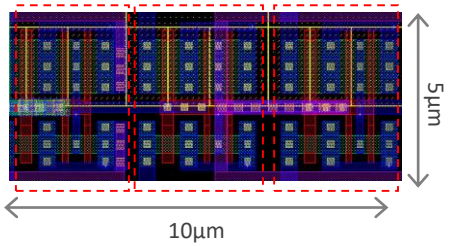
**CiAmps™ are fast, robust, and truly low power:**

- Frequency range is 100 times higher than conventional CMOS amplifiers,[2]
- Not slaved to threshold voltage nor process parameter variations,
- Can operate at extremely low power supplies as low as 10mV for the CiLNA™ or 100mV for the high-gain CiAmps™ (may be limited by other circuit elements such as supply voltage to turn on switches).

# CiFET™ CiLNA™ & Super-Sensor CiTIA

CiTIA™ / CiLNA™ core sensor circuits having controlled input resistance,
to maximally engage sensor energy

# Super Sensor in Single-Ended & Differential Configurations Including Self-Bias

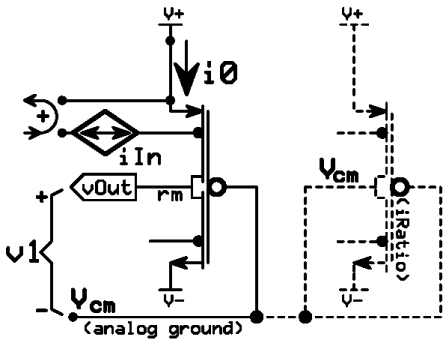
| Symbol | Schematic | Physical Layout | Description |
|---|---|---|---|
|  |  |  | **Single-ended high Trans-Impedance gain** (CiTIA™ Super-Sensor)<br>Self-biased by a CiFET™ these trans-impedance amplifiers are optimal for RF Low-Noise-Amplifiers, bus/transmission line receiver termination, and optical receivers as well as extracting energy from sensor devices with low noise and high gain/speed.<br>Example: $r_m$ = 0.7MΩ gain factor yielding $R_{in}$=5kΩ with 10mV PTAT/CTAT termination from an CiFET™ iRatio™ of 4 |
|  |  |  | **Differential High Trans-Impedance Gain** (dCiTIA™ Super- Sensor)<br>Low resistance is obtained by increasing the transistor size of the basic trans-impedance amplifier. Ultra-high frequency applications require a suitable layout access configuration with low impedance RF signal paths.<br>Note: For the same iRatio™ (4) the gain and differential input resistance double, plus the output swings twice as much. |

# Direct Conversion of CiFET™ iPort Input Current to Output Voltage

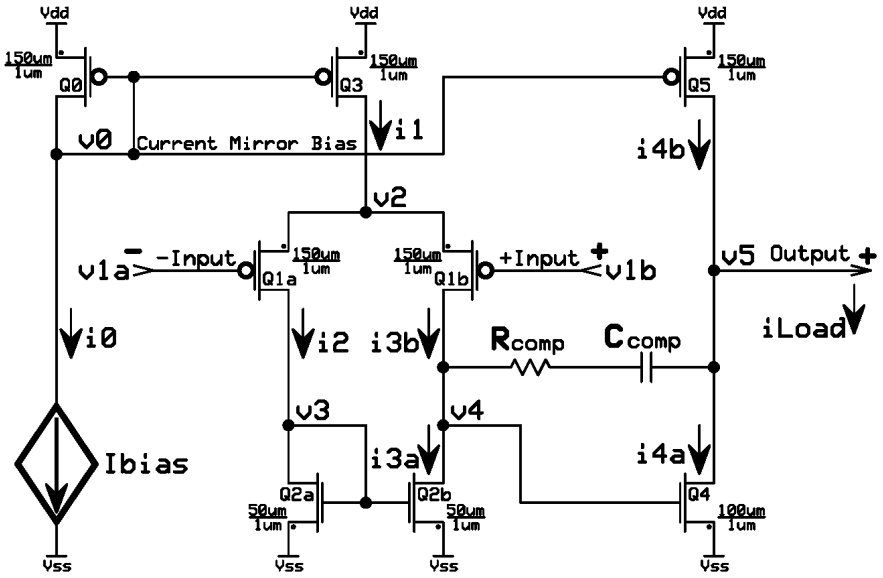
Analog Signal processing within a CiFET™ uses a direct conversion from iPort™ input current **iIn** to a low impedance output voltage **v1** with amplification by transimpedance gain $\mathbf{r_m}$ (1MEG for example). A change in iPort™ input current augments the CiFET™ bias current path **i0** which passes through all 4 CiFET™ channels that are operating under a common gate voltage. This common gate of the 4 CiFET™ channels constrain CiFET™ operation consistent with gate-to-source voltage solutions of all channels within the CiFET™ current path.

The individual CiFET™ gate-to-source voltages operate backwards from conventional intuition:
The common channel current forces the Vgs voltages instead of the conventional Vgs voltage controlling the drain current of the individual channels. These Vgs voltages are stacked between the same supply voltage that controls the gate voltage. This unique operating solution provides a direct CiFET™ output at the common drain node at low impedance for high-speed and low-noise operation.

**CiFET™**

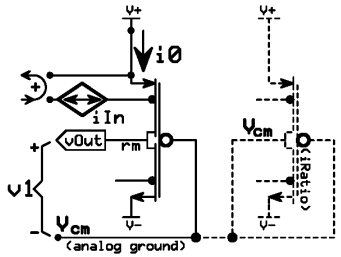



**Conventional CMOS OpAmp[6]**



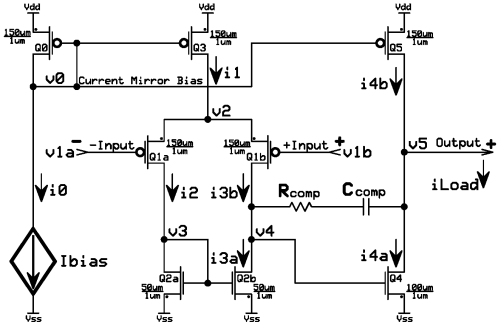
# Analog Signal Step-by-Step Conversion
# CiFET™ vs Conventional Operational Amplifier

## CiFET™ Operation




1. **Current → Voltage**: The CiFET™ injects iPort™ analog signal input current directly into the operating bias current passing through all channels of the CiFET™ in series to establish a low impedance output voltage directly by $\mathbf{r_m}$ without any incidental conversions back and forth between current and voltage.

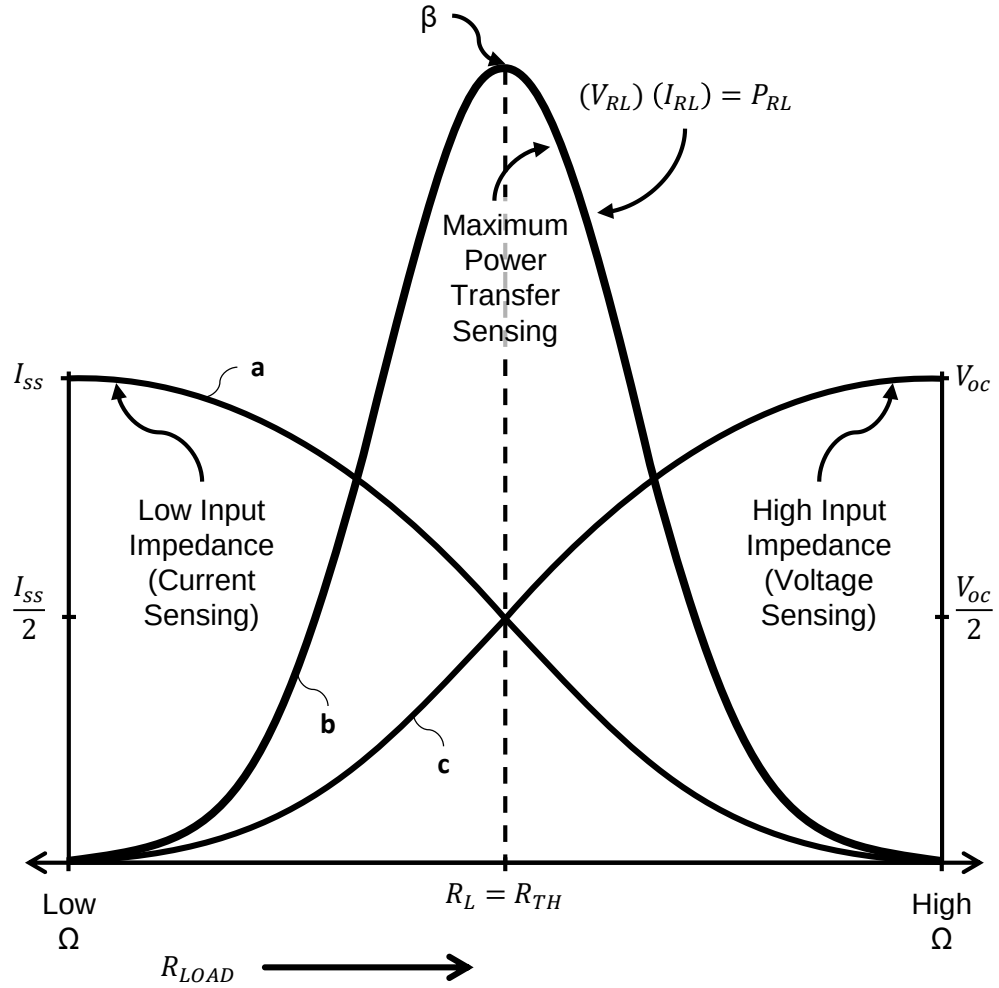
## Conventional CMOS OpAmp[6] Operation




1. **Current → Voltage**: Input bias current **i0** is converted to voltage **v0** by $\mathbf{g_m}$ of diode-connected **Q0**;
2. **Voltage → Current**: voltage is converted to a long-tail current by $\mathbf{g_m}$ of **Q3** and output pull-up current **i4b** by $\mathbf{g_m}$ of **Q5**;
3. **Voltage → Current**: Input voltage **v1a** is converted to current **i2** by $\mathbf{g_m}$ of **Q1a** and Input voltage **v1b** is converted to current **i3b** by $\mathbf{g_m}$ of **Q1b**; then
4. **Current → Voltage**: current **i2** is converted back to voltage **v3** by diode-connected **Q2a**;
5. **Voltage → Current**: voltage **v3** is mirrored to current **i3a** again by $\mathbf{g_m}$ of **Q2b**; and
6. **Current → Voltage**: current differences **i3a** & **i3b** are *subtracted* to form voltage **V4** to drive **Q4**;
7. **Voltage → Current**: voltage **v4** is converted to current **i4a** yet again by $\mathbf{g_m}$ of **Q4**; and
8. **Current → Voltage**: currents **i4a** and **i4b** are *subtracted* and applied to the output load resistance in parallel with the amplifier output resistance to form the ultimate output voltage **V5**.

***The CiFET™ replaces all of this with a single direct conversion from its input current to its low impedance output voltage with minimal time delay and almost no noise.***

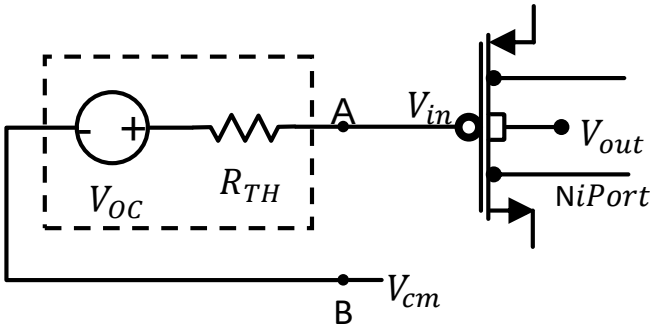
# Sensor Signal Enhancement by Sensor Energy Harvesting



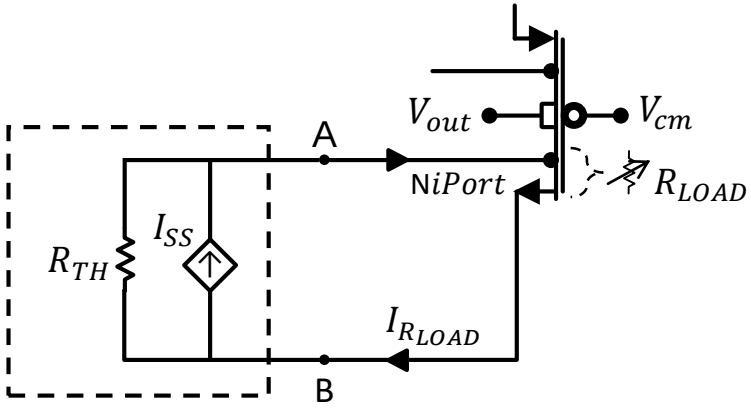

CiFET™ Signal Sensing Interfaces can be set to harvest maximum energy from signal sources at the electronic interface in order to capture maximum energy directly into the operating channels for obtaining maximum signal to noise ratio.
This plot illustrates the three classes of sensing by impedance matching:

1. Conventional high input impedance sensing "**c**" for high impedance signal sources;
2. Matching sensor impedance **"b"** and;
3. Low input Impedance sensing **"a"** such as RF LNAs where the CiFET™ input Impedance is set to a low value.

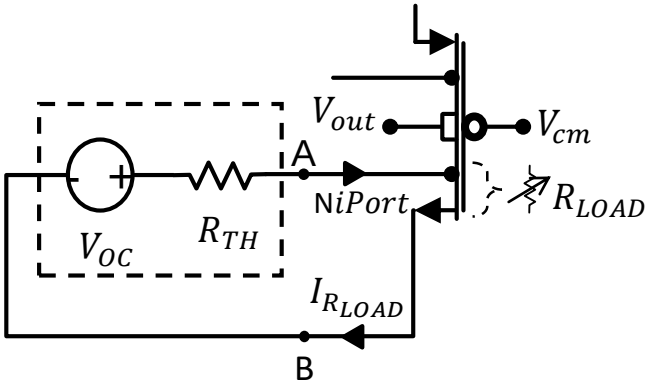
# 3 Cases of Maximum Sensor Energy Harvesting by CiFETs™




Conventional High-Impedance Signal Source Sensing by High-Impedance CiFET™ Gate Input Mode of Operation

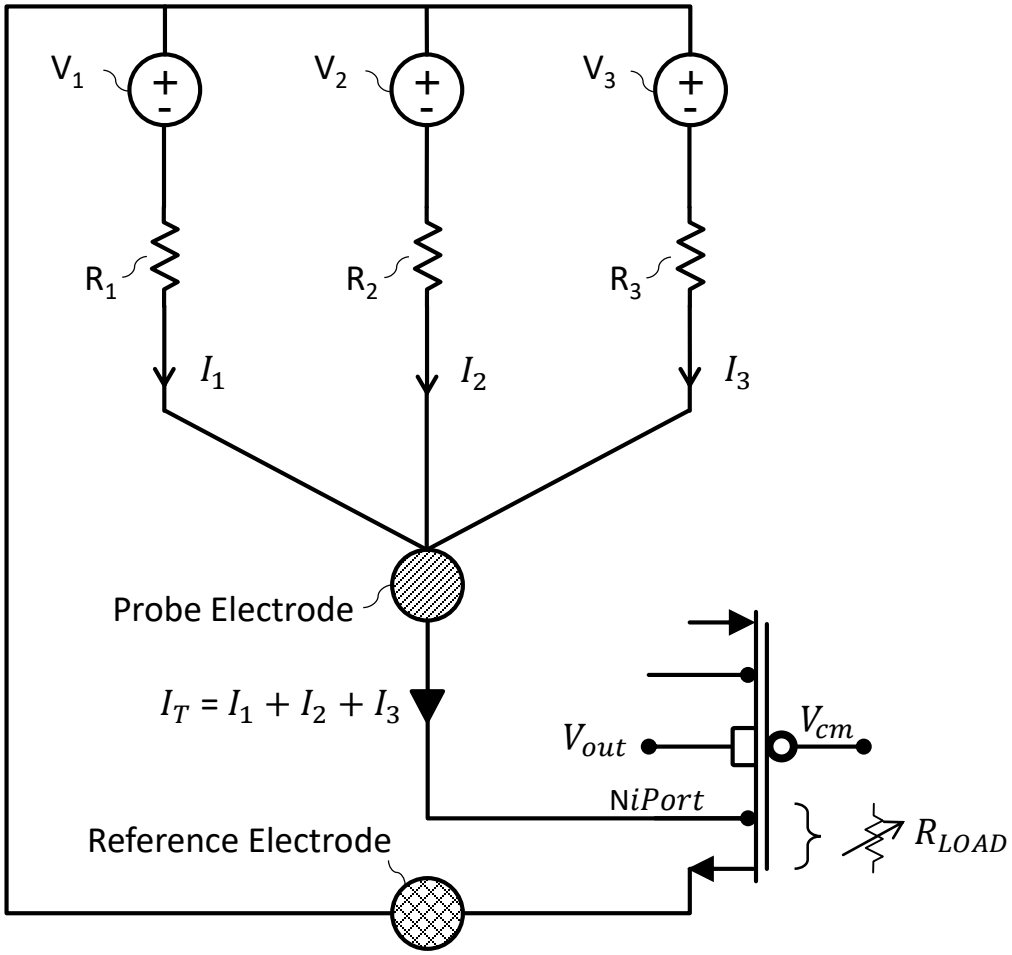



Medium Source Impedance Sensing by CiFET™ iPort™ Input Current Mode of Operation where iPort™ Rin is Matched to the Signal Source Resistance




Low Source Impedance Sensing by Maximizing Energy transfer into a Low Resistance CiFET™ iPort™

# CiFET™ Preferentially Emphasizing a Signal by its Source Resistance

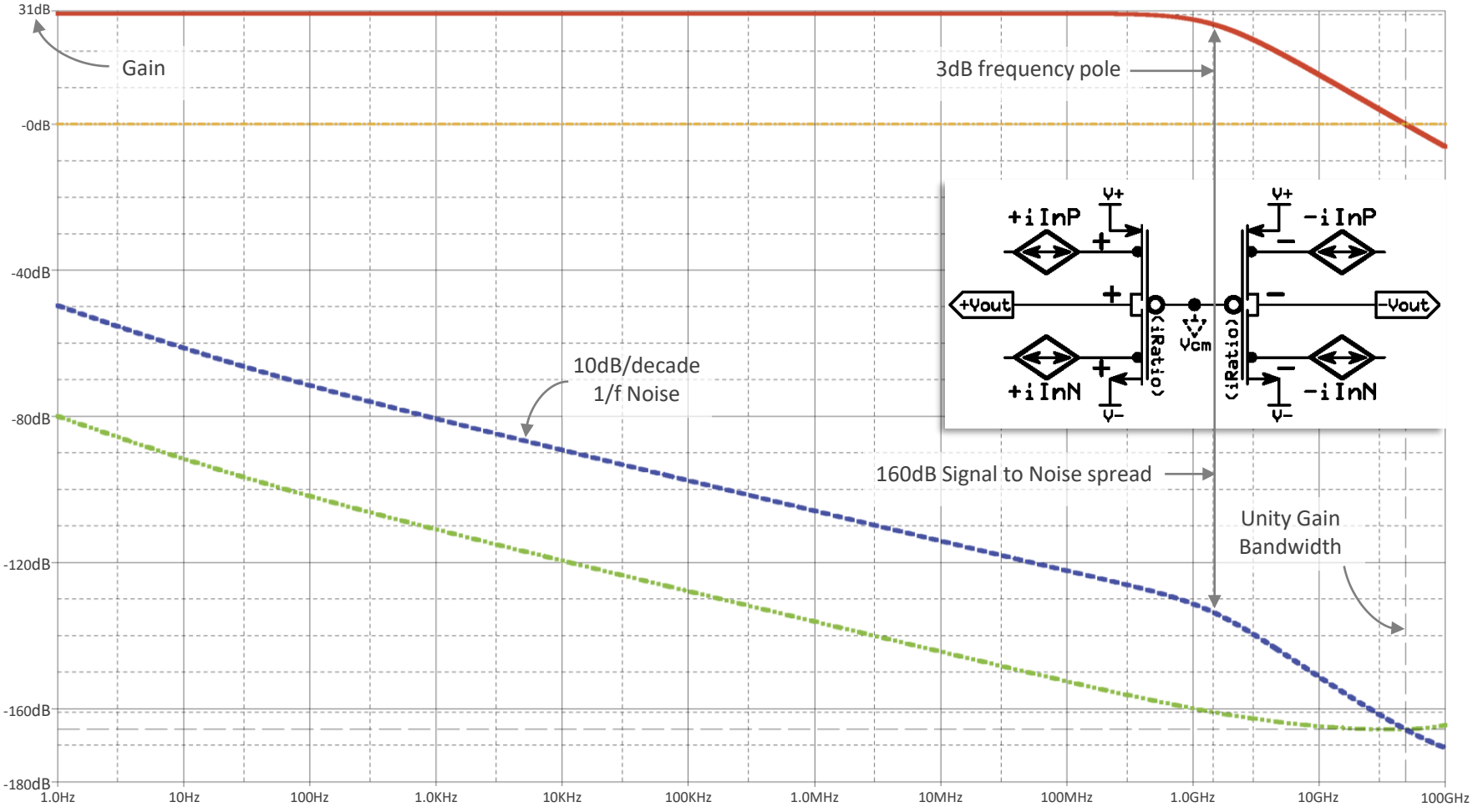



Identical signals can be preferentially emphasized by actively matching their distinctive Thevenin source resistance to CiFET™ iPort™ input resistance. If conventional bandpass filters could be used, similar signals would suffer severe distortion.

An example of this is preferentially selecting lower impedance heart activity from higher impedance more distant muscular noise and other environmentally coupled noise such as 60Hz powerline interference. With conventional high-impedance sensing, these signals are received at the same amplitude and in the same bandwidth.

# CiFET™ LNA

**Sensor Interface and Low Noise Amplifier (LNA) in 180nm Logic IC Process**
(Frequency scales with IC Process Ring Oscillator speed)




Full Differential 50Ω CiTIA™ Gain

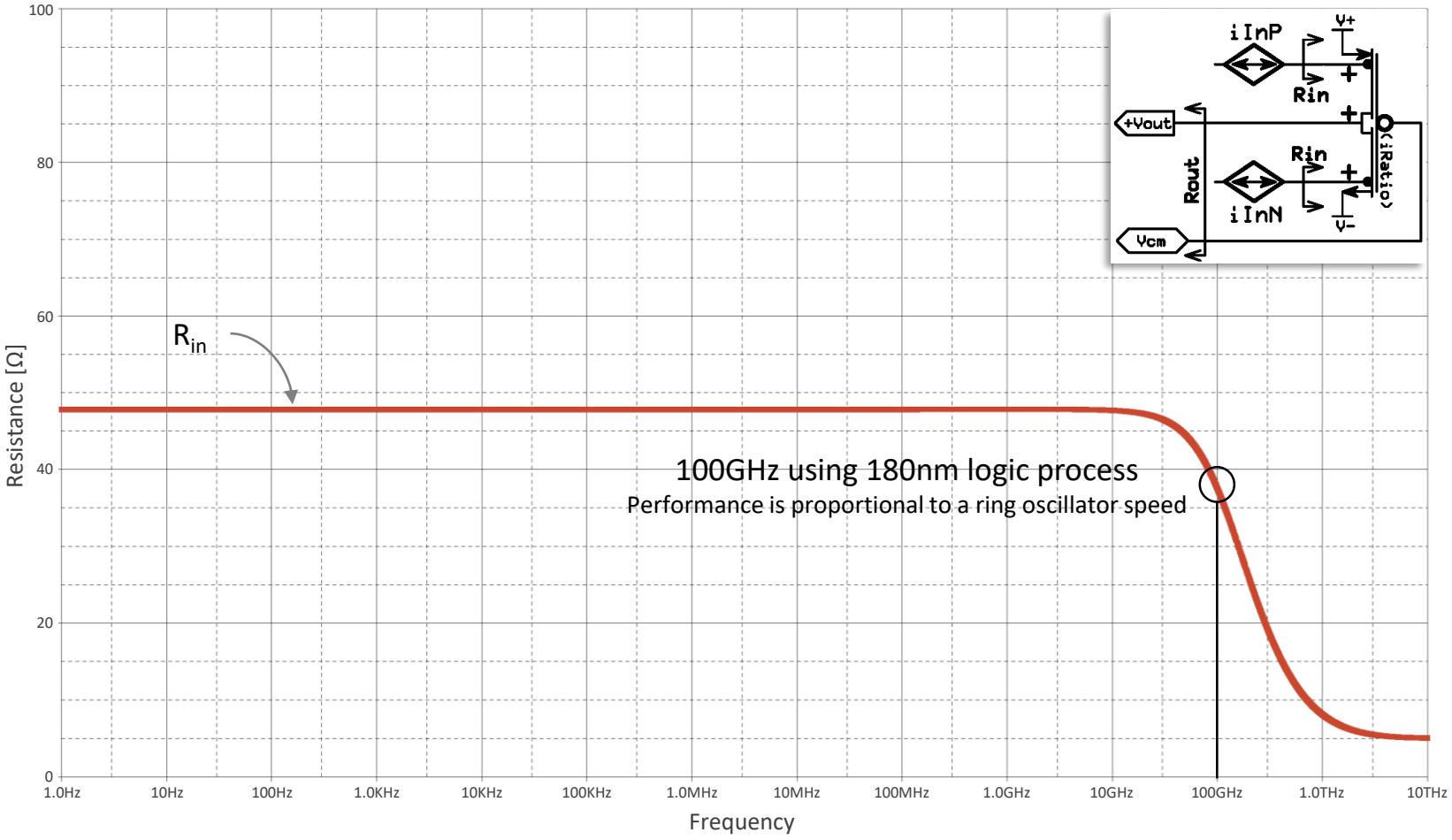
Total Output Referred Noise

Total Input Referred Noise

# Sensor & RF Termination Resistance

Sensor and RF termination resistance is the CiFET™ source channel which gathers all incoming energy generate an output voltage

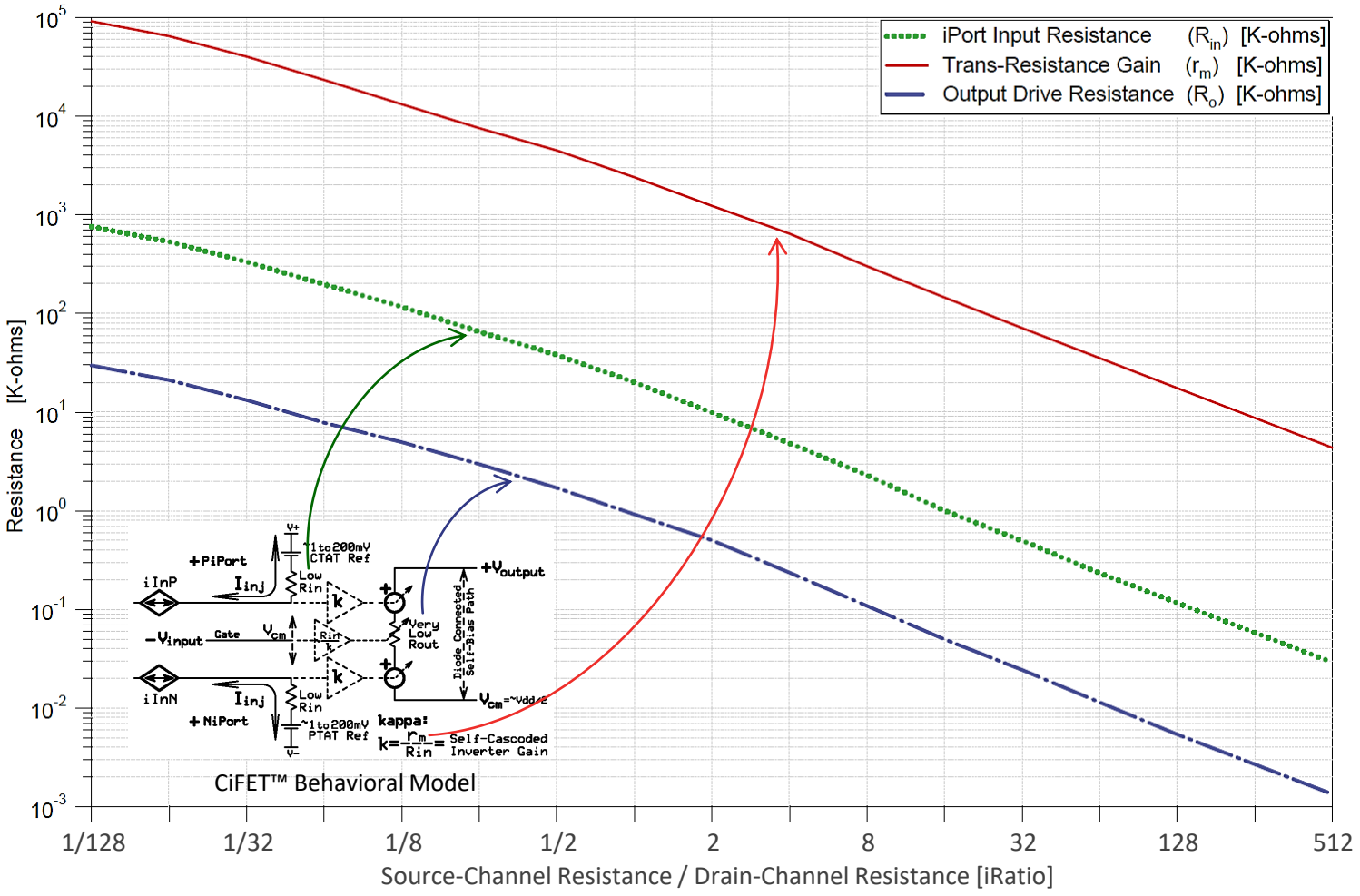
*Up to ~100GHz using 180nm process exemplified:*



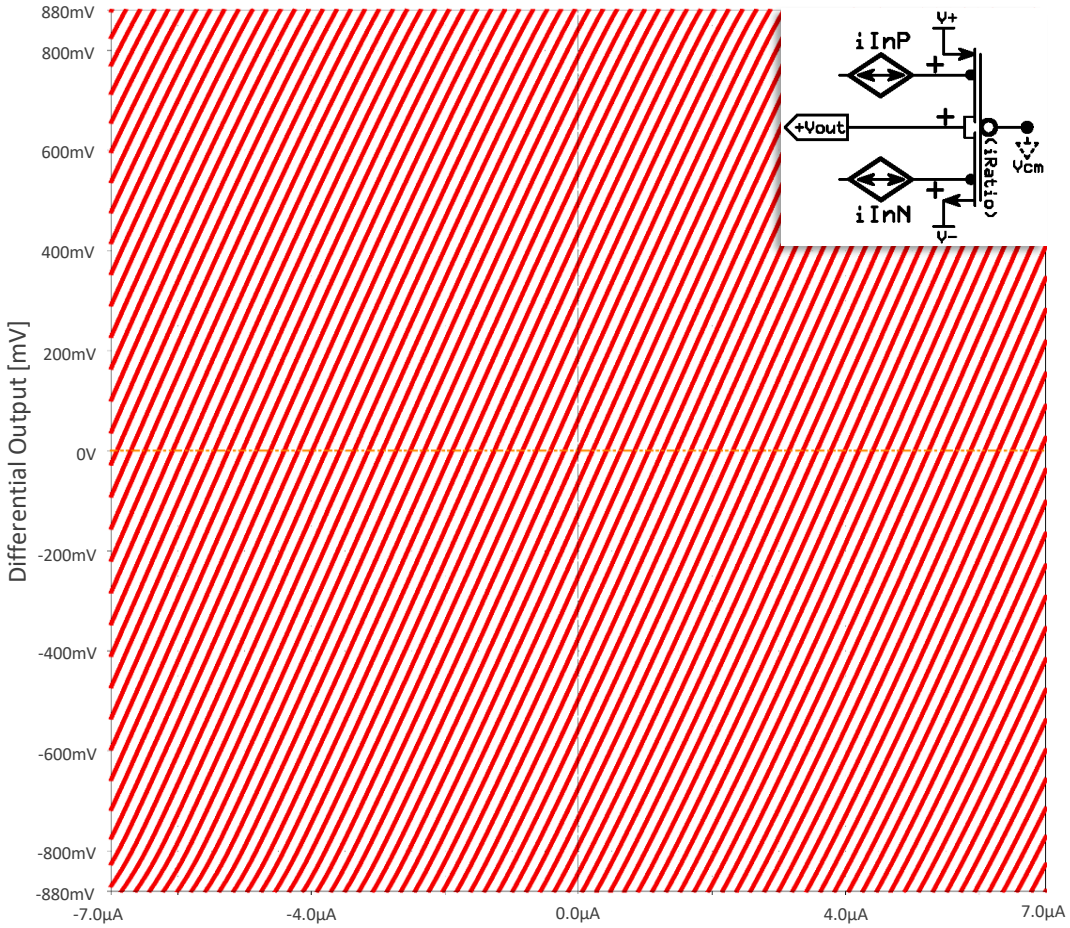
# CiFET™ as a Resistive Device

The CiFET™ can simply be considered a purely Resistive device: iPort input current into $R_{in}$ yields an output voltage equivalent to the input current going through $r_m$ but driven by a low (1/gm) drive resistance. The input-referred noise approaches that of the low Rin.

CiFET™ iPort Input Resistance ($R_{in}$) to Trans-Impedance Gain Factor ($r_m$) driven by Low Output Drive Resistance ($R_{out}$) Principal as a function of Intra-Channel Resistance-Ratio (iRatio)



# 4-Quadrant CiTIA™ iPort Modulation



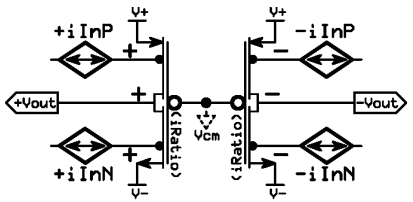

4-Quadrant Additive iPort™ Linearity Plot

CiTIA™ as an instrumentation PiPort™ + NiPort™ signal adder — illustrates ultra-precise 4-quadrant linear relationship between iPort™ inputs through sweeping one iPort™ while the other iPort™ is stepped for each successive sweep over the entire linear ± dynamic operating range.

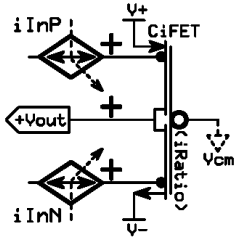
With a differential CiTIA™ having 4 iPort™ inputs, 4 input signals can be modulated onto the same output. Another summing method is to wire-or multiple current inputs into any of the iPorts™.

All 4 iPort™ inputs are active with the Trans-Impedance gain set to 125KΩ*2 by an CiFET™ iRatio™ of 4 with a Vsupply=1.8 volts resulting in the same iPort™ scale.

**Alternate Differential CiTIA™**

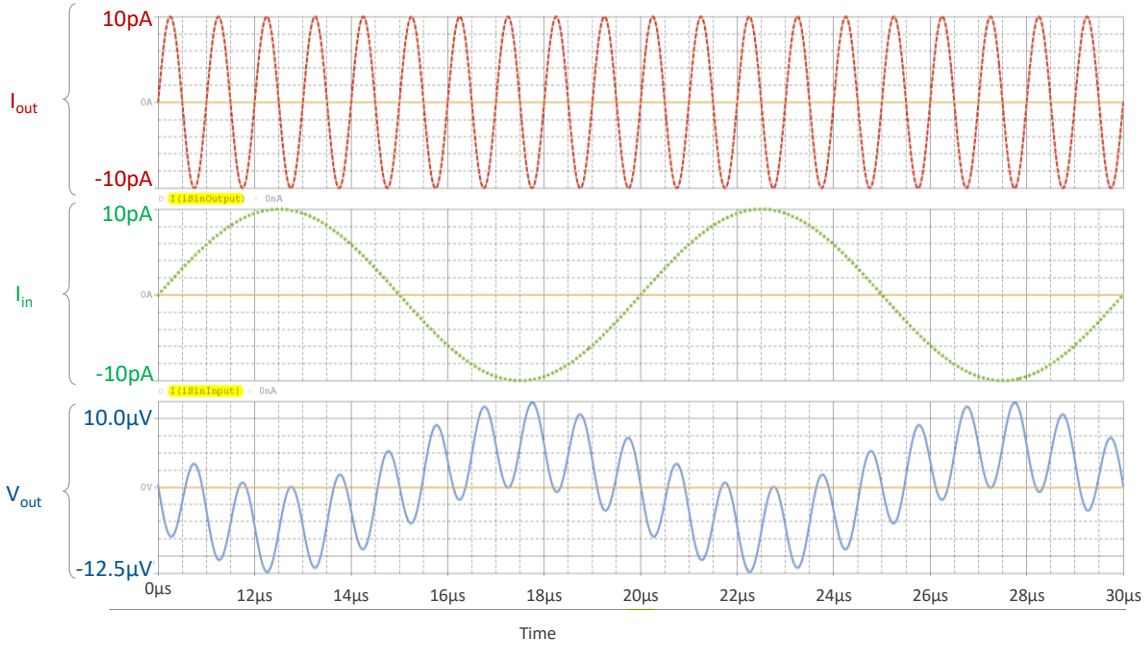


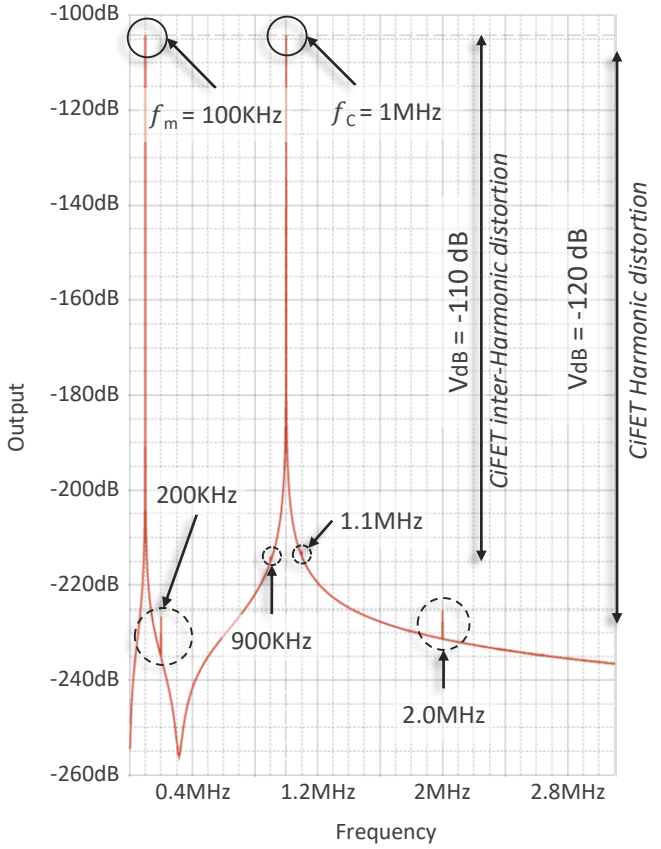
# CiFET™ Spectral Purity



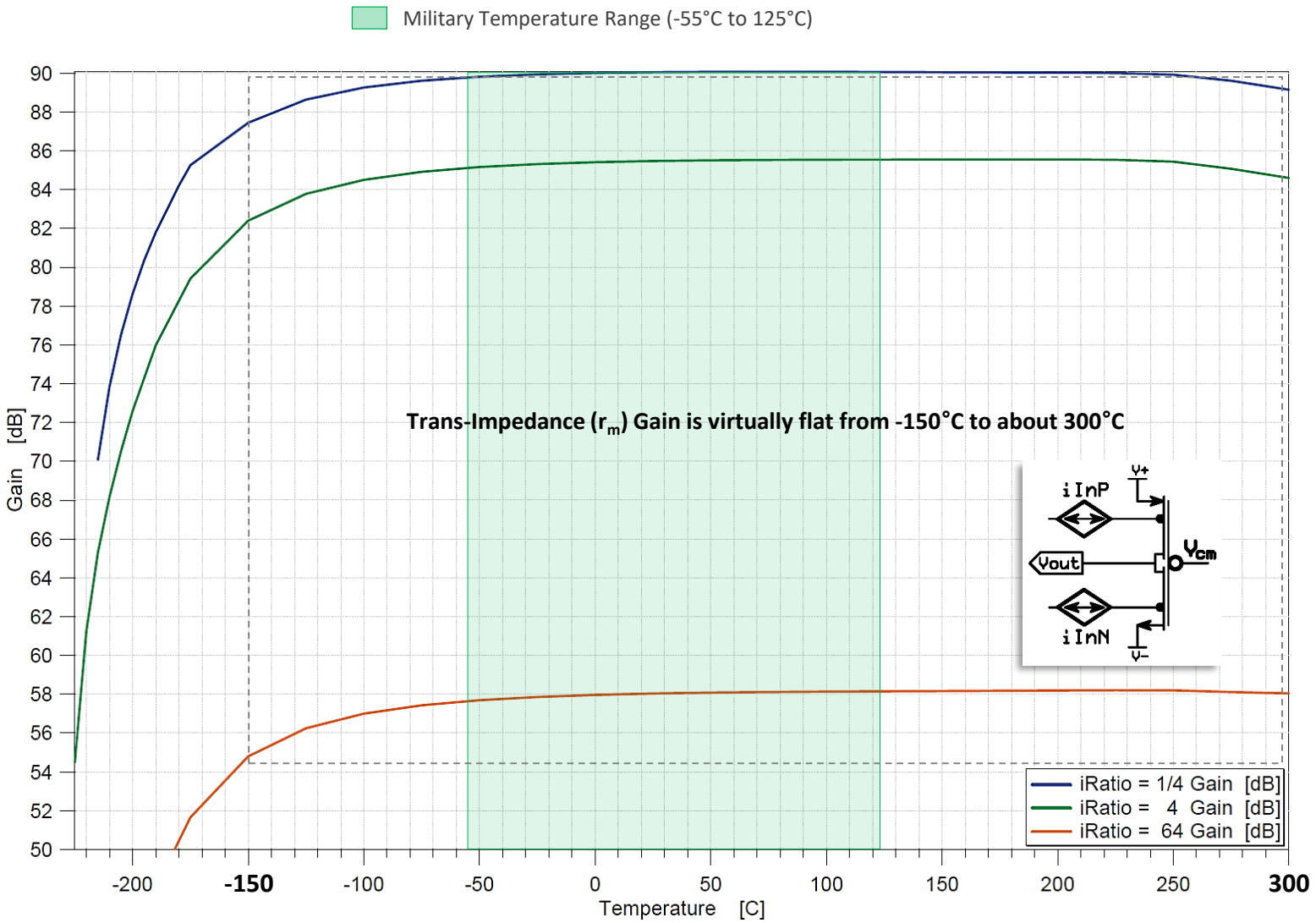

Modulation by addition of two separate sine waves imposed on the two iPort™ inputs, provide a precisely modulated output having unprecedented spectral purity, thus expressing CiFET™ PPM level of linearity.

Spectral Purity of 2 Sine Waves Summed by PiPort™ + NiPort™ (iRatio™ = 4)
$f_C$=1MHz (Carrier Frequency), $f_m$=100KHz (Frequency Modulation), $V_{DD}$=1.2, 180nm process node



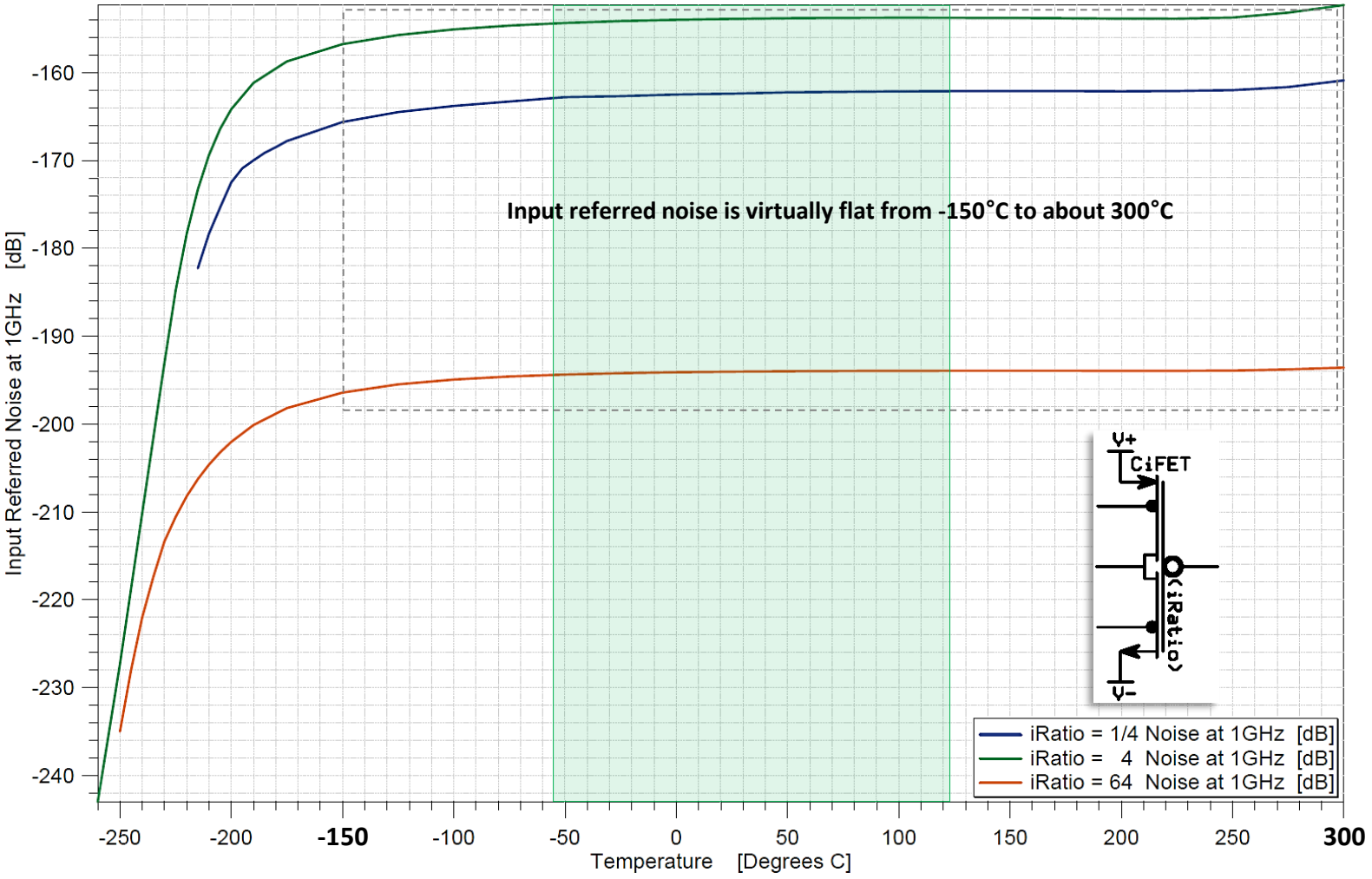
# CiFET™ - Temperature [°C] vs. Trans-Impedance ($r_m$) Gain [dB]




Low temperature properties are the availability of free impurity electrons or holes in the semiconductor while high temperature floods the semiconductor properties with thermally-free carriers, as opposed to conventual high threshold voltage at low temperature and leakage current at high temperature

# CiFET™ - Temperature [°C] vs. Input Referred Noise at 1GHz [dB]

Low Temperature limited by NO electrons in the conduction band and high temperature limited by ALL electrons in the conduction band.
Radiation hardness similarly benefits from the iRatio™ imposed parametric insensitivity.



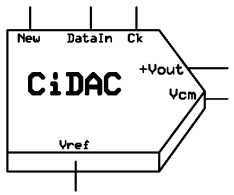

Military Temperature Range (-55°C to 125°C)

# CiFET™ Some Application Examples

A few illustrative examples of CiFET™ circuit applications
to illustrate performance and flexibility

# 16-bit CiFET™ Digital-to-Analog (CiDAC™)

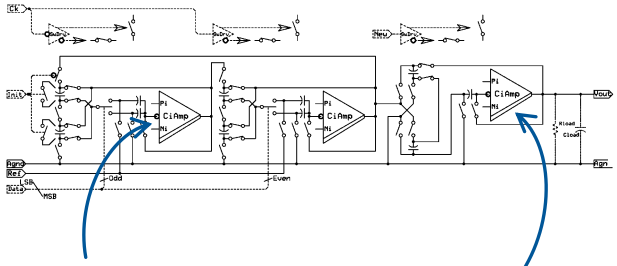
**Single-Ended DAC**




Possible to achieve 20-bit resolution (1-PPM accuracy of 1µV/Volt) due to linearity and gain of CiFET™ amplifiers within the constraints of kTC capacitor noise

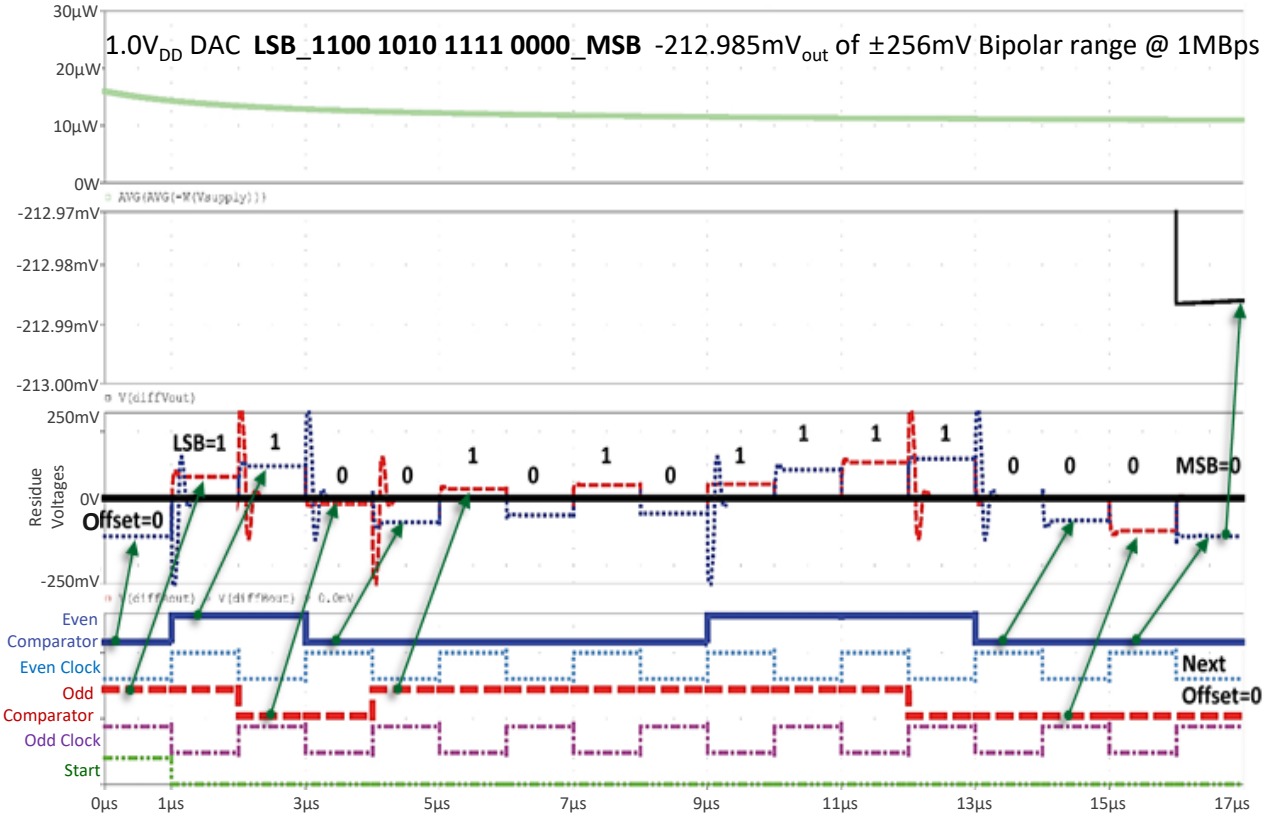
**Successive Approximation DAC**

2-stages recirculate 8 times for 16-bits and feed output sample and hold for a complete DAC



Two 1-bit DAC stages recirculate n/2 times

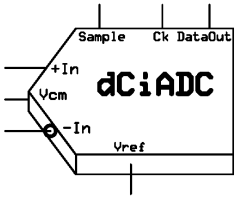
Optional Output Hold




Digital bit input sequence is reversed → LSB first to MSB last.
Output voltage dynamic range was set to -255mv to +256mv (4µV/DN) instead of the normal 1.024 volt (16µV/DN) dynamic range to illustrate higher resolution capability.

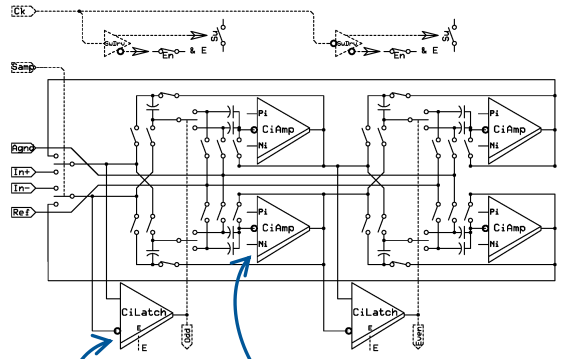
# Full-Differential 16-bit CiFET™ Analog-to-Digital (dCiADC™)

**Differential ADC**



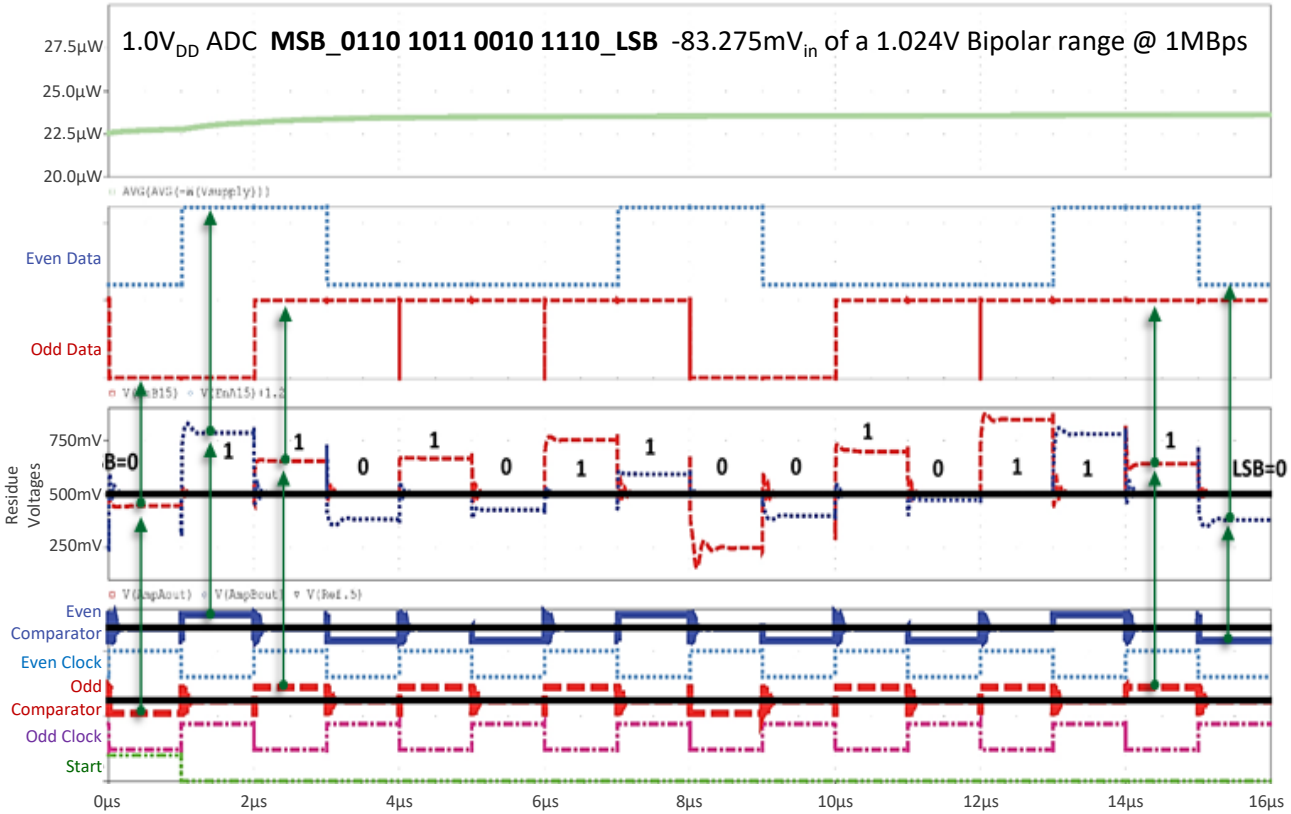

Possible to achieve 20-bit resolution (1-PPM accuracy or 1µV/Volt) due to linearity and gain of CiFET™ amplifiers within the constraints of kTC capacitor noise

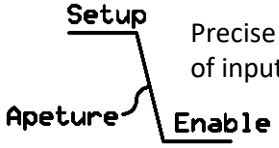
2-stages recirculate for 16-bit resolution




Comparators

Two 1-bit ADC stages recirculate n/2 times

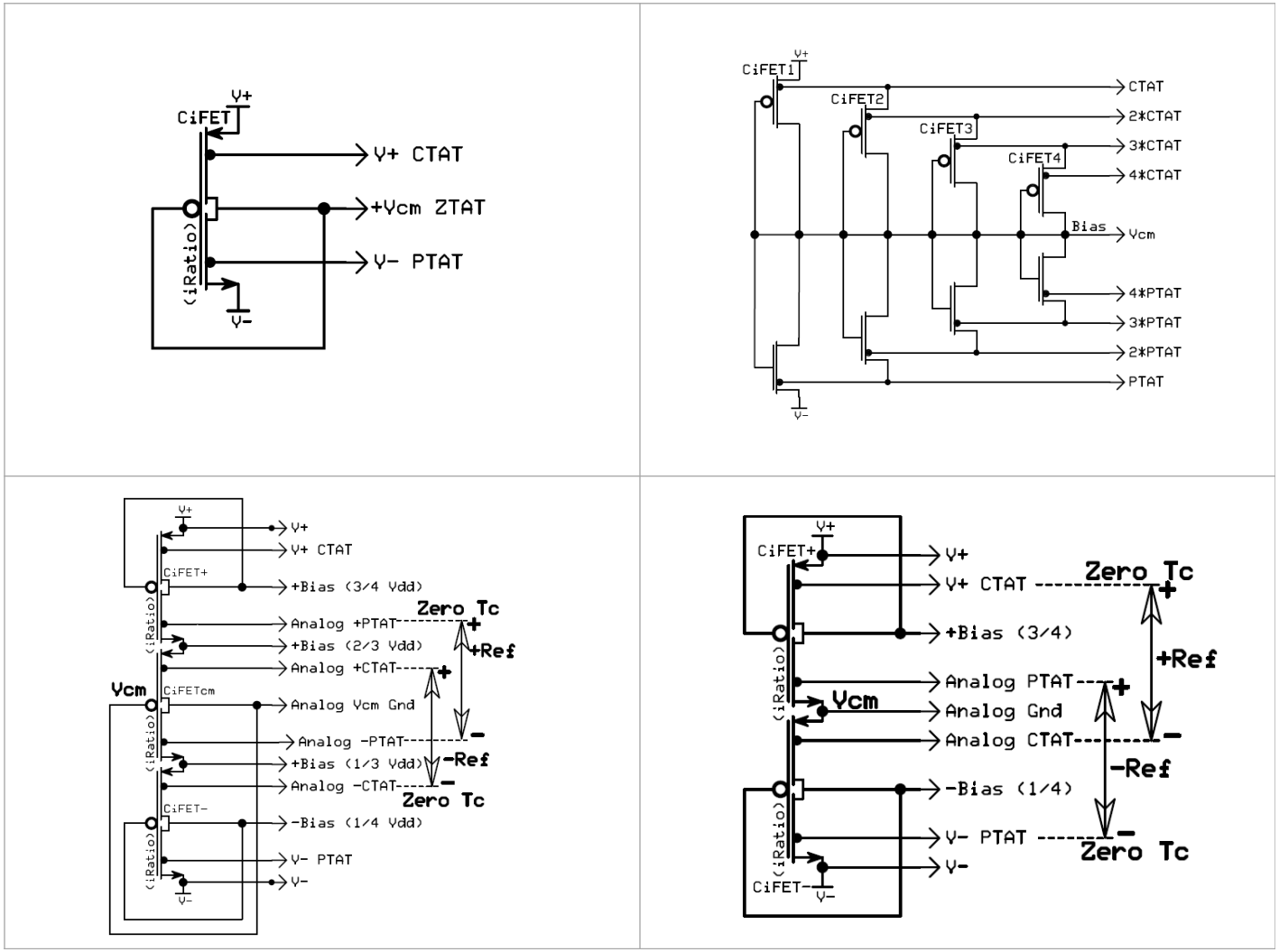


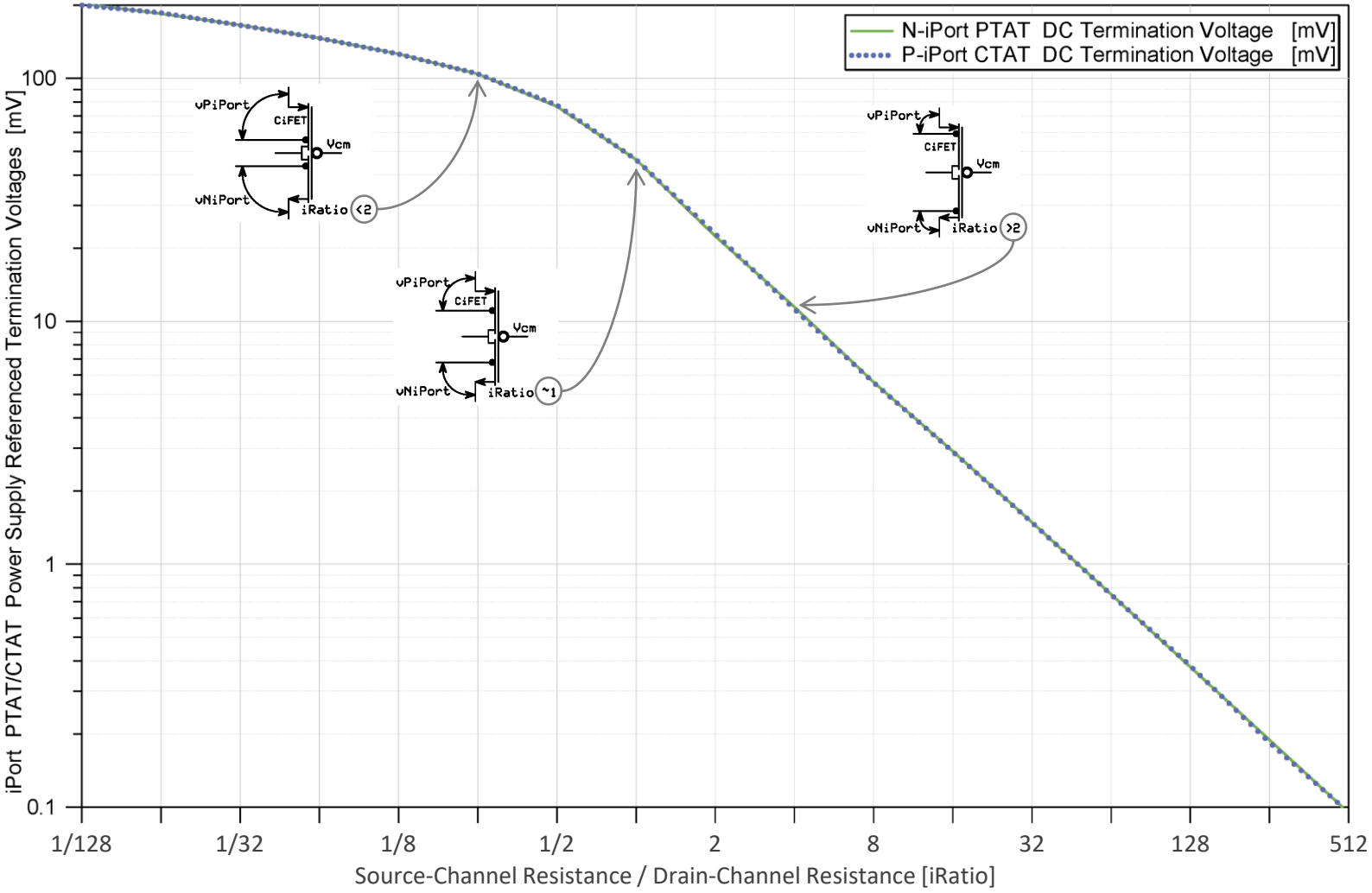

Precise S&H aperture time samples independent of input voltage level with bottom plate sampling

# CiFET™ Voltage Reference Examples (PTAT & CTAT)

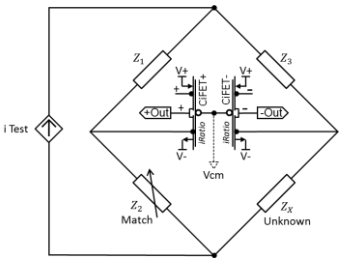
Reference voltage generator related to analog virtual ground (CiFET™ self-bias) or supply voltage



# iPort™ Termination Voltages (PTAT & CTAT) vs iRatio™

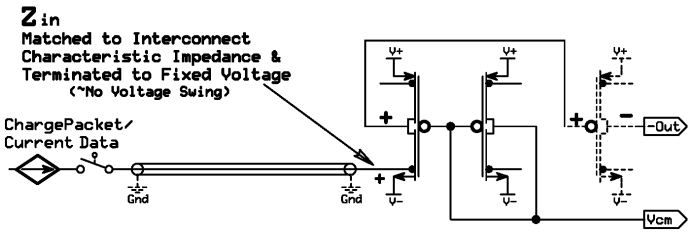


# Additional CiFET™ Transimpedance Amplifier Sensing Applications



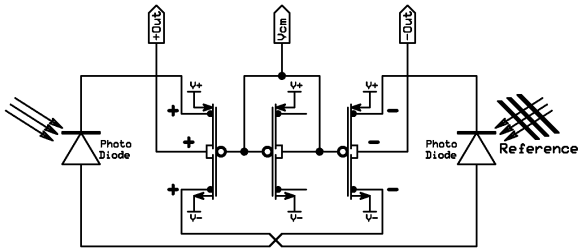

### CiTIA™ Wheatstone Impedance Bridge Sensor

A four-terminal bridge can be developed with a high input impedance with respect to the bridges impedances, or it can be designed to be a differential current balanced sensor.



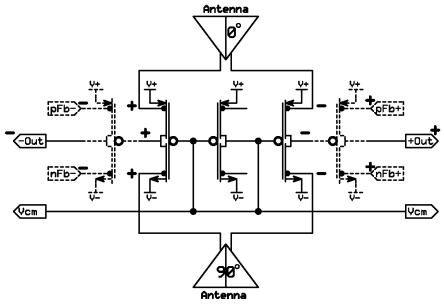

### CiTIA™ transmission line/bus wire receiver

Bus or transmission line termination energy is absorbed and reused in the CiFET™ super-saturated channels which are locally referenced, eliminating ground noise while low I/O impedances provide high speed ~without parasitic loading.




### CiTIA™ fiber-optic receiver

Receiver photo-diodes are self-biased and sensed by a low resistance to efficiently extract optical signals at wide bandwidth. Extra series CiFET™ stages can be added to provide additional gain.

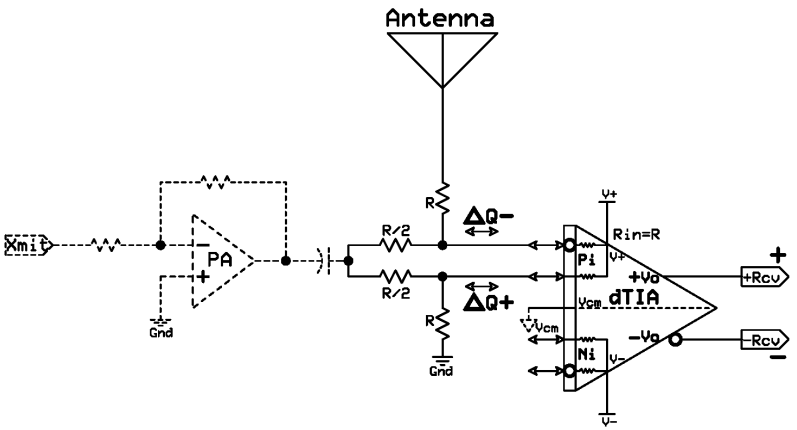



### CiTIA™ dual summing antenna CiLNA™ with additional gain and filter port/feedback access

Complementary Trans-Impedance Low Noise Amplifier can isolate, terminate, and sum one or two antennas at extreme high frequencies with PPM linearity and ultra low noise while providing resistive filter input ports in optional second stage (dotted).

# Concurrent Transmit & Receive Phase Array Antenna Element

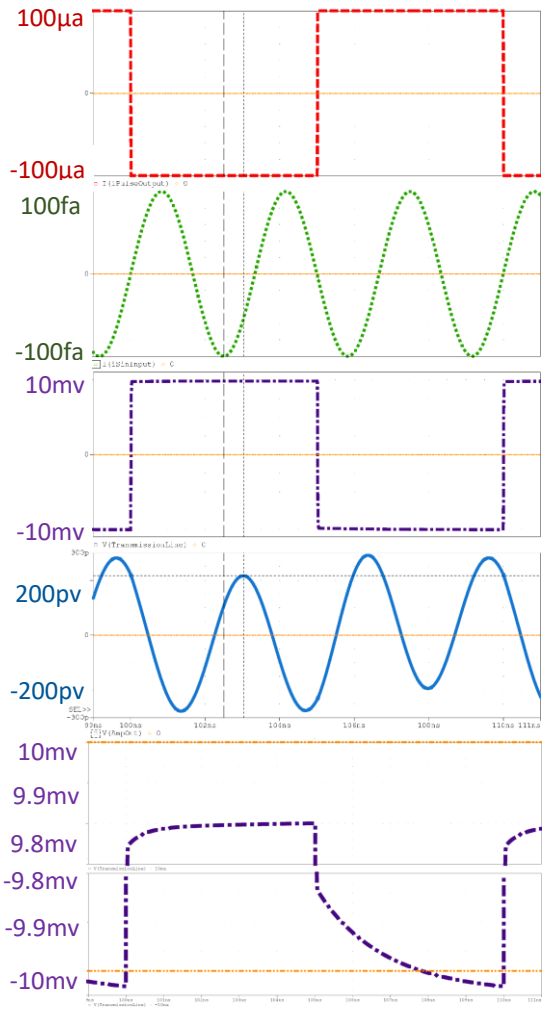
**Full-differential CiTIA™ Isolator**




Differential Isolator[4] built as dCiTIA™ separating an infinitesimal 10pv (=100fa) 300MHz sine wave downlink signal from a 10 decade stronger concurrent 10mv (=100µa) 10ns [100MHz] pulse uplink. No restriction to signal content and frequency; even exactly the same downlink and uplink waveforms are valid.

Here the antenna of the dCiTIA™ Isolator is driven by a 100uA pulse uplink signal by the Power Amp (PA) while concurrently receiving a smaller downlink sinewave signal on the same antenna. The composite antenna signal voltage is the middle purple waveform, with its magnified top and bottom regions as the lower magnified waveform set. The solid blue received sinewave is the amplified downlink, which on the verge of crosstalk at the 10 decade signal difference.

Isolating **10 decades** of signal amplitude



# Circuit Seed Inventors

- **Susan Schober** has a Ph.D. in Electrical Engineering: Analog IC Design, as well as the following degrees; Master of Science in Biomedical Engineering, Certificate in Technology Commercialization, Master of Science in Engineering Management, Master of Science in Electrical Engineering, Bachelor of Science in Electrical Engineering
- Her research interests include creating novel, low power circuits for deep sub-µm CMOS technologies, developing phase locked loops (PLLs) for multi-GHz frequency synthesis, and the physical characterization and modeling of high frequency RF devices
- Taught analog IC design at USC (class of 2016 rated #1 by students)
- (6) publications and (15) honors and awards to date
- Contributed to (7) patents and more than (20) patent applications in process to date

- **Robert Schober** is an accomplished entrepreneur with 50+ years of experience and a groundbreaker in ultra-low power circuit design
- As an Electrical Engineer by profession he has worked for General Electric, Lockheed, TRW, Hughes, American Hospital Supply, & JPL
- Performed analog and digital design and layout of analog and digital systems up to and including custom microprocessors, direct memory access controllers and floating- point processors as well as many spacecraft instruments
- Designed and implemented most types of data converters, and other analog circuitry, including ultra-low power biomedical analog to fast multiple-giga-sample flash mode Gallium-Arsenide Analog-to-Digital Converters and numerous Radio Frequency integrated circuits
- Initialed the first CMOS image sensor DARPA project at JPL, first blood oxygen sensor, first neural stimulator, first integrated circuit pacemaker leading to implantable defibrillators, and many other breakthrough devices
- Holds multiple patents in the areas of cardiac pacemakers, high efficiency/compact digital integrated circuit cell libraries, RF and high sensitivity RFID integrated circuits, as well as multiple patent applications in the area of endoscopic pill cameras

- **Herbert M. Shapiro** was a critical catalyst for the IP group at Bell Laboratories for 27 years
- He prepared and prosecuted in the U.S. Patent and Trademark Office patent applications covering software, lasers, optics, magnetic card readers, power supplies, power strips, transmissions, avionics, medical devices, document scanners, printers, fiber optics, semiconductor devices, semiconductor processing equipment, solid state cameras, hydraulic systems, flat panel displays, telecommunication systems, electronic circuitry, RFID systems, etc.
- Very-first MOS patent, first bubble memory patent, first IC RF inductor, among many other firsts
- Advanced degree in what became solid-state physics from Rensselaer
- Filed over about 1000 approved patents including the original MOS patent by William Shockley
- Has over 10 personal patents issued and others presently applied for


Circuit Seed™

www.CircuitSeed.com

# References

[1] Reducing Variation in Advanced Logic Technologies Approaches to Process and Design for Manufacturability of Nanoscale CMOS – Kelin J. Kuhn, Intel;

[2] An Introduction to On-Chip Variation (OCV) – AnySilicon Feb 28, 2017;

[3] Transistor Aging Intensifies at 107nm and Below – Ann Steffora Mutschler, executive editor, Semiconductor Engineering, July 13th 2017;

[4] Low Frequency Circulator and Isolator Uses No Ferrite or Magnet, Charles Wenzel – winner of 1991 RF Design Awards Contest;

[5] Semiconductors II-Doped transport slide presentation (used Page 6 to correlate with the wide and flat temperature performance); http://www.ee.sc.edu/personal/faculty/simin/ELCT563/03%20Semiconductors%20II-Doped;%20transport.pdf

[6] On the Design and Characterization of Femtoampere Current-Mode Circuits – B. Linares-Barranco & T. Serrano-Gotarredona, IEEE JSSC, v38, #8, Aug 2003.

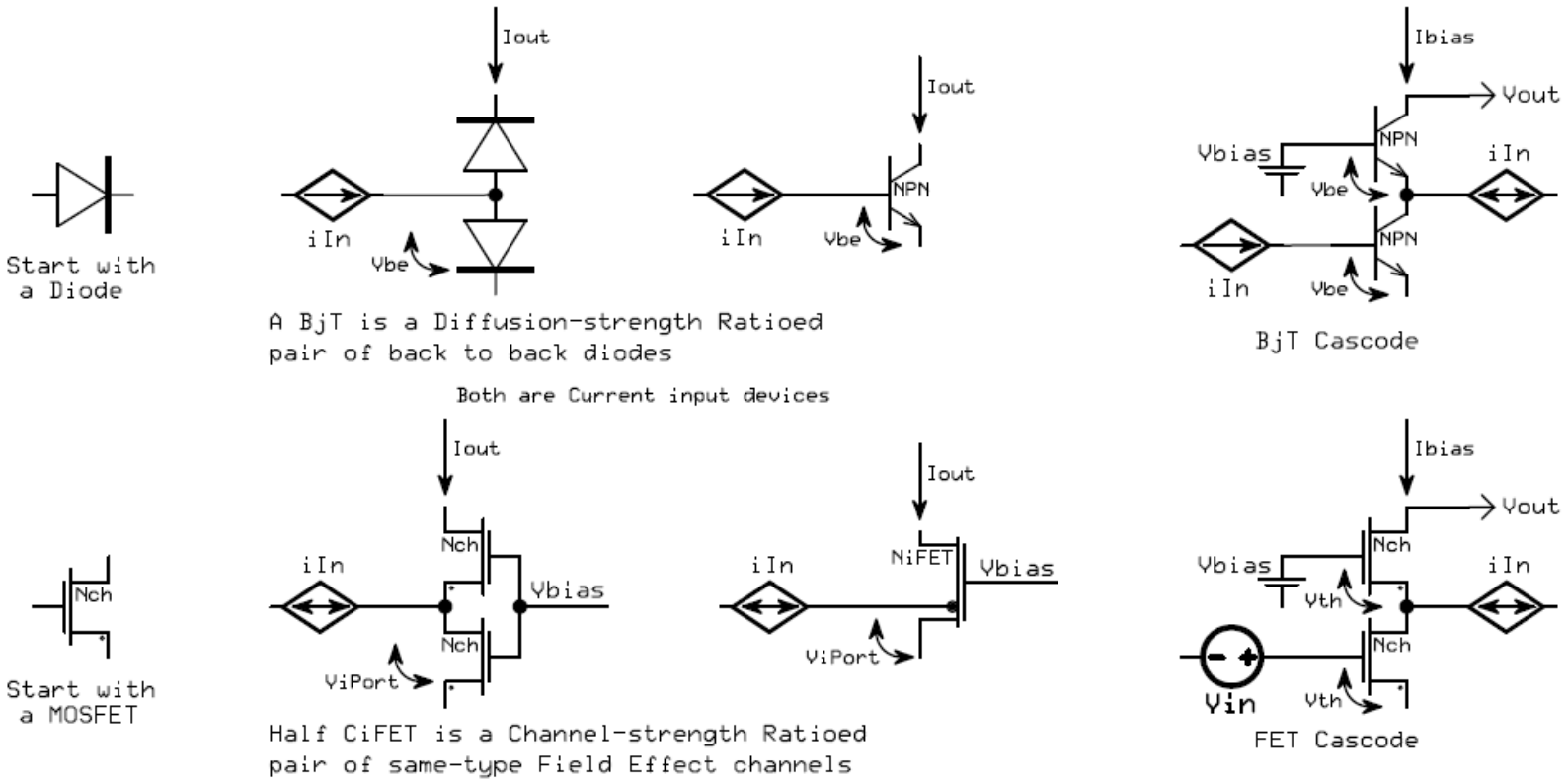
**For more details, please contact:**

**Keith Taylor**
*Vice President Acquisition & Licensing*
ktaylor@inventionshare.com
(613) 225-7236 Ext. 135

# Appendix

## Reinventing the transistor in any nanoscale CMOS logic-only IC process

CiFET™ is a fusion of MOSFET channels similar to the BiPolar transistor being fusion of a pair of diodes.
Both derive their functionality from the relative properties of the individual parts.

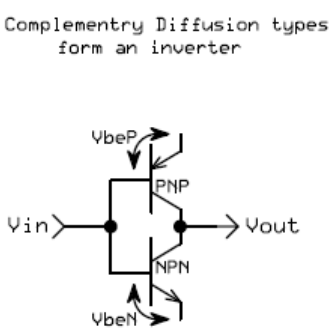



**The CiFET™ is a multi faceted device that functions as both a device and a circuit concurrently**

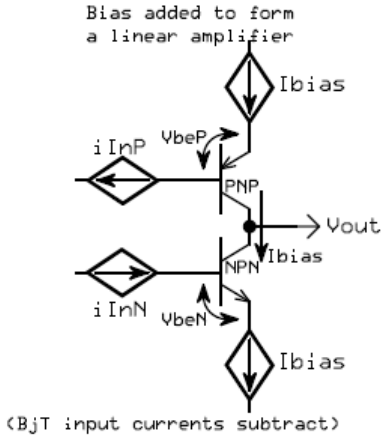
# Appendix

## Reinventing transistor Amplifiers in any nanoscale CMOS logic-only IC process

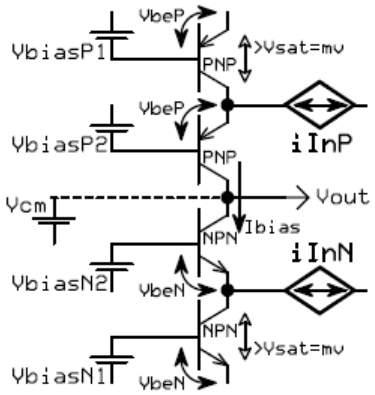
CiFET™ 4-Quadrant operation about its self-generated common mode voltage (ac ground) without cross-over distortion
(all inputs and outputs go equally in either direction or can be left at zero if not used)



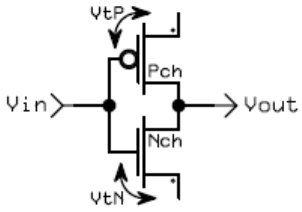

~BjT Inverter



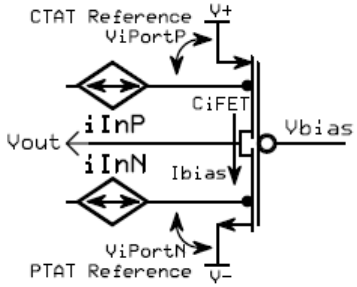

BjT Push-Pull




Complementry BjT Cascode

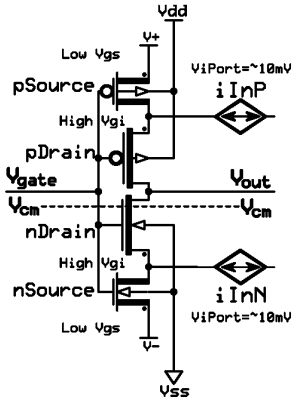



CMOS Inverter



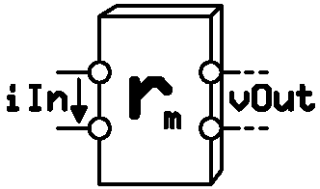

(CiFET iPort currents add)

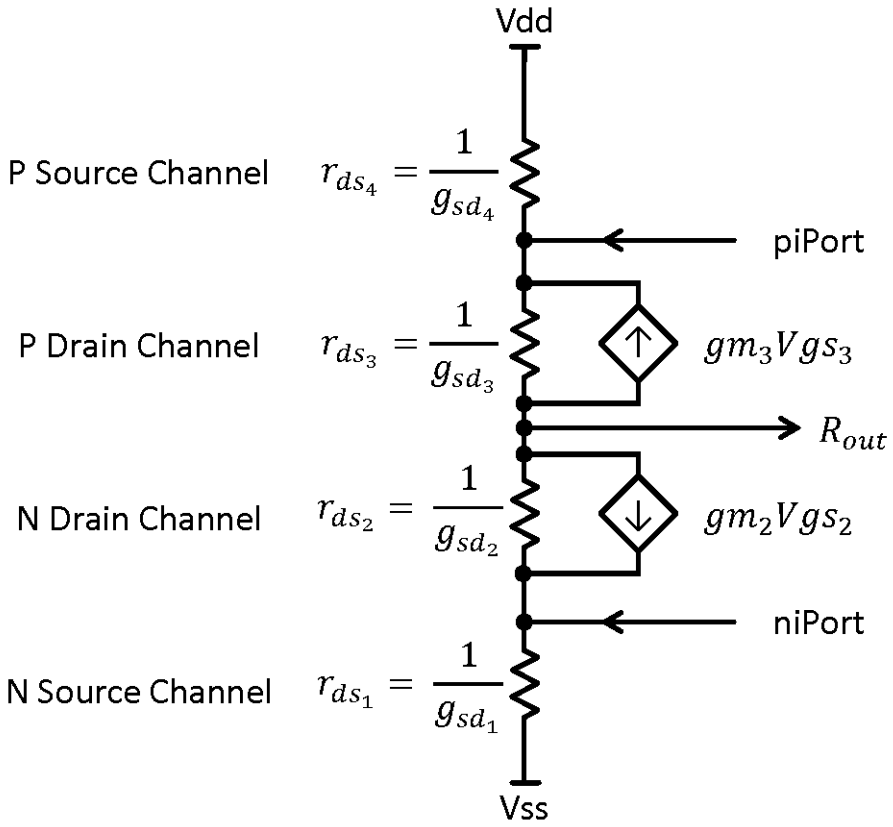
CiFET




CiFET Self-Cascoding

# CiFET™ Mathematical Model



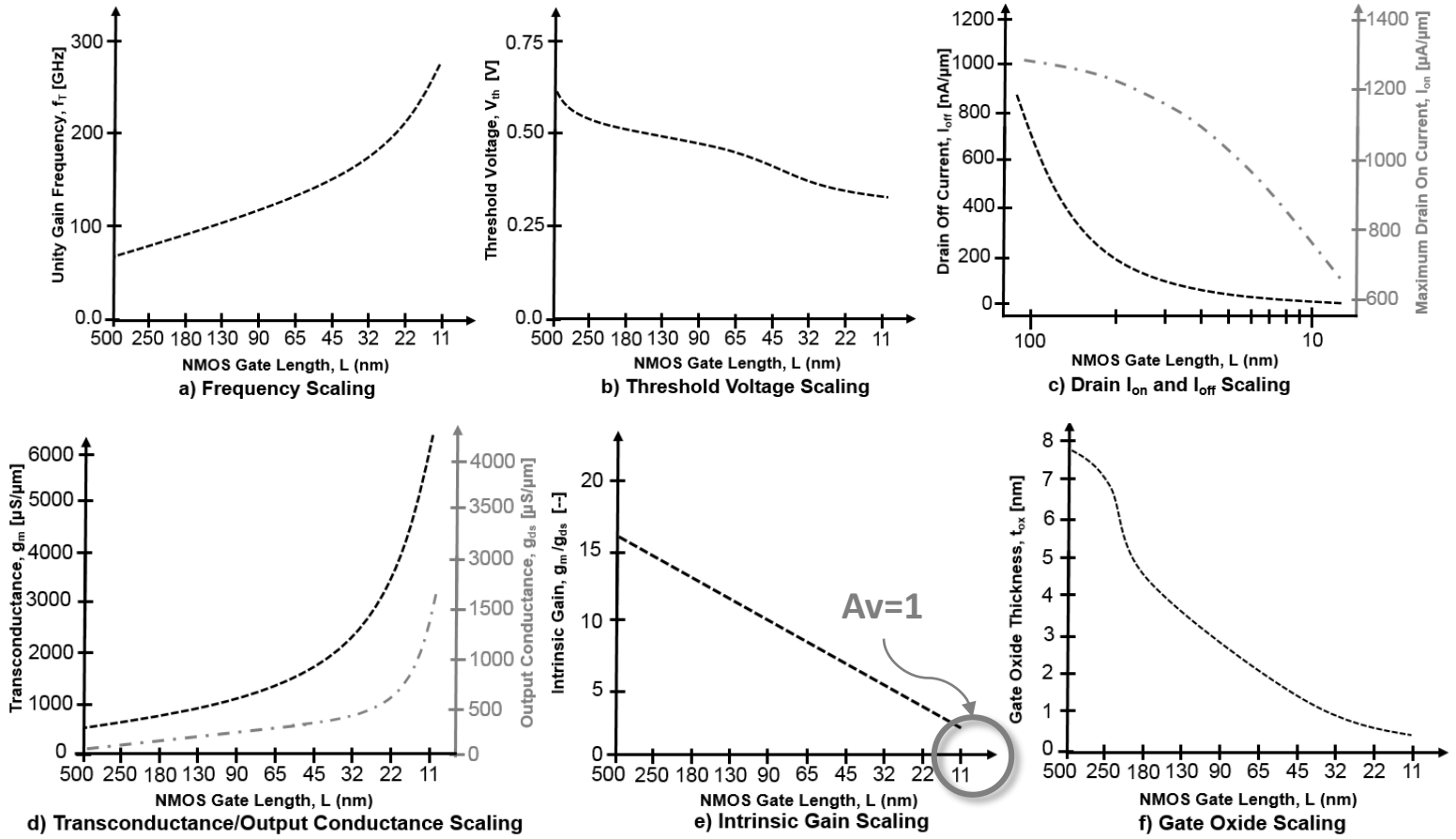

The iPorts see source-channel resistive termination to their respective power rails for their current inputs

The drain channels work like common-gate amplifiers to provide gain with their input voltage at their iPorts

# Appendix

## A new Emerging Limit to Scaling MOS Analog Design Parameters

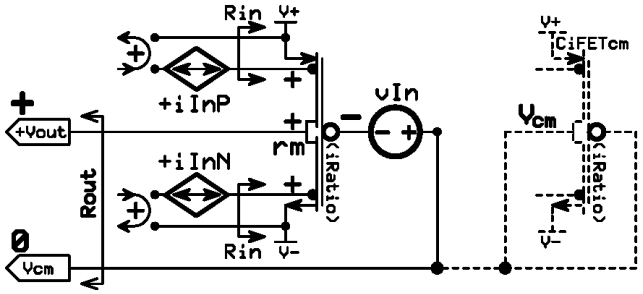
Intrinsic Gain shrinks to *Unity* near the 5nm IC process node (Plot e)




Pertinent analog design parameters are plotted against IC process node size to reveal their interrelationship. **Plot d)** shows the much desired transConductance-gain increasing dramatically as process' shrunk, but on the same plot d) the output conductance increases progressively faster. As **plot e)** output conductance ($g_{ds}$) reaches 1/2 of the transconductance ($g_m$), intrinsic gain ($g_m/g_{ds}$) approaches unity, revealing that analog will not be practical at nanoscale. Long channel pinch-off output resistance is required for conventional high output resistance $g_m*R_L$ analog voltage gain.

# Additive CiFET™ Sensor interfaces in Single-Ended & Differential Configurations Including Self-Bias

**Single-ended high Trans-Impedance gain**
(CiTIA™ Super-Sensor combined with its high impedance voltage input)




**Differential high Trans-Impedance gain**
(dCiTIA™ Super- Sensor combined with its high impedance voltage inputs)