A charge transfer-based high performance, ultra-low power CMOS charge pump for PLLs

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Abstract This paper presents a novel high performance, ultra-low power scalable CMOS charge pump (CP) design for analog phase-locked loops (PLLs) fabricated in all-digital nanoscale IC processes. The compact CP circuit uses four minimally-sized transistor switches and a relatively small capacitor for transferring charge within the PLL to adjust the voltage controlled oscillator frequency in the PLL control loop. Unlike the state of the art designs, the proposed CP topology does not use current mirrors, nor does it suffer from traditional mismatch errors due to its unique structure. Additionally, this charge transfer-based CP has the ability to operate at very low supply voltages well below 1V. The fast switching action of the proposed CP allows for the use of a no-added delay D-flip flop-based phase-frequency detector resulting in a reduced PLL control loop delay and very low reference spurs in the overall PLL design. The proposed CP has been placed in a 0.5-10GHz PLL, fabricated, and physically tested in an all-digital 40nm TSMC CMOS process. Additionally, post-silicon measurements of the CP circuit have been completed with a variable 0.2-1.2V supply and a 50MHz-1GHz reference frequency. The proposed charge pump has an active area of 0.0004mm^2, consumes on average 250pW power, and has a 0.1-0.3^o phase error, dependent on the PLL frequency of operation.

Keywords Charge pump · Phase-locked loop · PLL · Frequency synthesis · Ultra-low power analog ICs · Low supply voltage · Charge transfer · nanoscale · CMOS

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1 Introduction

The phase-locked loop (PLL) is a ubiquitous control system used for precise frequency and phase generation, clock synchronization, and signal recovery. For multi-GHz wireline and wireless integrated circuit (IC) applications there are two primary PLL design approaches: 1) analog and 2) digital. Generally, analog PLLs, such as the charge pump PLL (CPPLL) block diagram shown in Fig. 1, have a larger IC footprint and can be more power hungry as compared to their digital phase locked-loop (DPLL) counterparts. On the other hand, DPLLs typically possess more complicated circuitry, are generally limited to frequencies significantly below 10GHz, and have a tendency to suffer from digital noise due to quantizing issues. In recent years, analog PLLs have incrementally adopted scalable digital circuit elements to their constituent blocks (e.g. dividers, phase detectors, and oscillators) which typically perform analog functionality with less area and power.

To date, a digital circuit component for every block in the analog PLL has been created except for the charge pump (CP) circuitry; this is due to the analog process extensions (e.g. current mirrors which require large transistors and voltage swings) that have been necessary to design this particular block using state of the art methods. The use of conventional CP designs and present lack of innovation for this circuit block has been a significant bottleneck in making analog CPPLLs scalable to and between nanoscale CMOS technologies for use in next-generation devices [1-9]. This work aims to advance the state of the art analog PLL designs by introducing a scalable ultra-low power, compact, and precise charge pump circuit. Presented in detail is the CP design for PLLs, along with transient, stability, and noise analyses, a brief discussion of the charge pump's recommended implementation in an all-digital nanoscale multi-GHz PLL, and the results of physical testing of the fabricated CPPLL and charge pump designs.

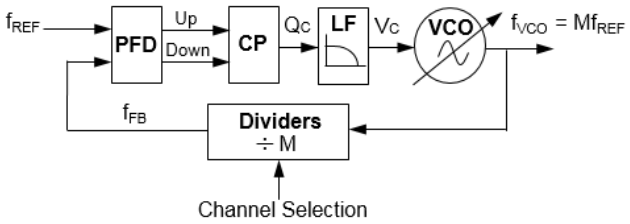

Fig. 1 Block diagram of a state of the art analog charge pump PLL [2]

2 Charge pump PLL overview

The main purpose of the charge pump block in a PLL is to control the output frequency of the VCO, f_{VCO}, by means of the control voltage, V_c. The voltage inputs to the CP are Up/Down error signals generated by a digital phase-frequency detector (PFD). When not idle, output of the CP is the charge, Q_C, which is converted to the control voltage, V_C, via the loop filter (LF) circuitry and stored on its effective capacitance, C_L, as seen in Fig. 2. Raising or lowering V_C will result in an increase or decrease of f_{VCO}, dependent on the oscillator design. The VCO output frequency is continually divided down by a preselected value, M, by the divider block and fed back into the PFD as the feedback frequency, f_{FB}. If any difference between the frequency and/or phase of the reference frequency and the feedback frequency is detected, an appropriate error signal pulse is generated by the PFD which is fed to the CP.

2.1 The charge pump in the PLL control loop

A typical closed PLL control loop operation would begin with the VCO in Fig. 1 producing f_{VCO} at phase, ϕ_{VCO}. This output frequency is divided down by an integer (or fractional value) to a lower feedback frequency, f_{FB}, that is comparable to that of the stable reference clock. The stable reference frequency, f_{REF}, and its phase, ϕ_{REF}, is then compared to f_{FB}, and phase, ϕ_{FB} in the PFD. If there is a difference in frequency and/or phase between the reference and feedback signals, the PFD produces the appropriate Up or Down error signal for the duration of the frequency or phase difference. In this work, an Up=logic 1 error signal is produced by the PFD when the ϕ_{FB} lags behind ϕ_{REF} and a Down=logic 0 error signal is given when ϕ_{FB} leads in front of ϕ_{REF}. When the PLL is in phase lock (i.e. $f_{FB}=f_{REF}$ and $\phi_{FB}=\phi_{REF}$), no error signal is produced (i.e. Up=Down=logic 0) and the loop is essentially in a steady state condition, also known as Idle mode.

In state of the art charge pumps, the values and duration of the PFD Up/Down error signals determine the action of the CP. For example, Up=logic 1 causes the applicable transistor switches (e.g. S_b in Fig. 2) of the CP to close allowing charge to be placed on the LF's C_L, for the duration of the Up signal, effectively raising V_C and consequently f_{VCO}. On the other hand, a Down=logic 1 input signal causes the opposite behavior in the CP to occur by closing the other relevant switches (e.g. S_a in Fig.2) and taking charge away from C_L, for the duration of the error signal thus lowering V_C and f_{VCO}.

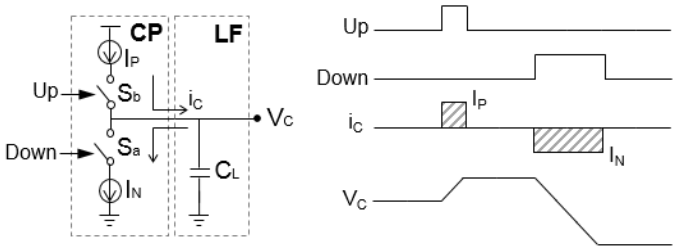

Fig. 2 State of the art PLL charge pump switch-based model and general characteristics [1-2, 6-8]

2.2 State of the art PLL charge pump challenges

State of the art PLL charge pumps such as the single-ended examples shown in Fig. 3, employ bulky current mirrors (i.e. I_N and I_P) and relatively large transistor switches (i.e. S_{a-d})—both of which are difficult to fabricate in nanoscale CMOS technologies—which flow substantial amounts of current linearly to and from the LF to alter V_C. Although this is effective, these CPs have significant design concerns including: 1) wasted static power due to current mirrors and biasing always working even during PLL phase lock (Idle mode), 2) large transistor switch W/L ratios are required for low voltage drop over the switch to enable maximum V_C swing (ideally rail-to-rail), 3) additional delay circuitry must be added to the PFD in order to allow the currents, I_P or I_N, time to stabilize after switching, 4) extra matching circuitry for the CP Up/Down output signal transitions is necessary for symmetric charge up and charge down as shown in Fig. 3(b), 5) analog process extensions (i.e. precisely matched current sources, large transistors, amplifiers) are extremely difficult to shrink to nanoscale CMOS technologies and generally very sensitive to process variation, 6) V_C output errors can easily occur (e.g. jitter, dithering) due to undesirable leakage current slipping through the transistor switches, thus affecting the VCO frequency when in phase lock, 7) limited headroom due to stacked transistors restricts use at lower supply voltages, and 8) relatively large active area [1-8]. The proposed charge pump described in the next section was designed in such a way as to overcome these challenges.

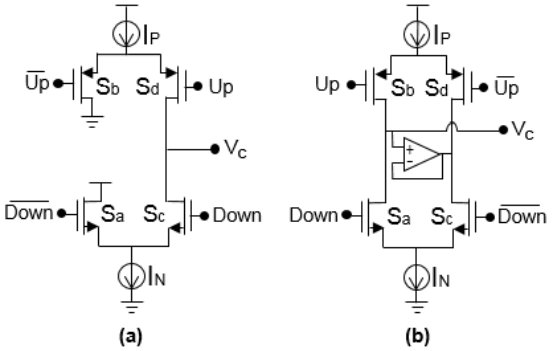

Fig. 3 Transistor-level schematic examples for (a) a basic state of the art CP and (b) a state of the art CP with matching circuitry [1, 6]

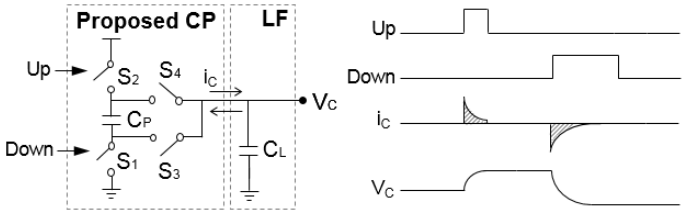

Fig. 4 Proposed PLL charge pump switch-based model and general characteristics

3 The proposed PLL charge pump

The proposed PLL charge pump shown in Fig. 4 is a new single-ended, capacitive charge transfer-based design that uses four minimally-sized transistor switches (i.e. $S_{1\text{-}4}$) and a relatively small metal interconnect capacitor (i.e. C_P). There are no analog process extensions, current mirrors, or large matched transistors, as in the state of the art designs. The transistor-level realization of the proposed CP design is shown in Fig. 5. This CP circuit uses the same inputs (i.e. Up/Down logic error signals from the PFD) and has a similar overall general result as the state of the art CPs in that the VCO frequency is successfully controlled, yet there are a few marked differences including the architecture, how the charge is transferred and held, the output voltage behavior, and total power consumption.

3.1 Operation

As with any PLL charge pump, there are three explicit switching modes of operation: 1) Idle, 2) Pump Up, and 3) Pump Down. The three following sub-sections describe each of these modes in detail for the proposed CP in the PLL control loop while highlighting the unique output voltage and current behavior and the amount of energy transferred for each mode, which is necessary to find the total dynamic power consumed while the CP charges and discharges in the various modes.

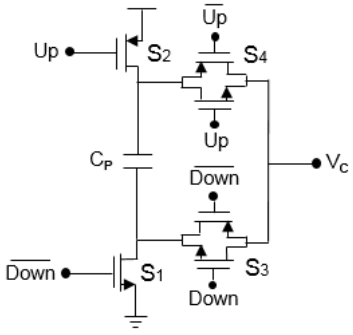

Fig. 5 Transistor-level schematic realization of the proposed PLL charge pump

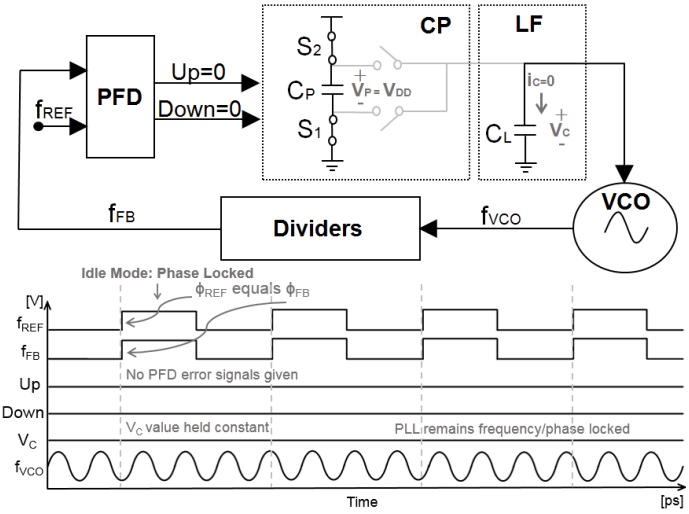

Fig. 6 Idle mode for the proposed PLL charge pump

3.1.1 Idle mode

Fig. 6 illustrates the switch view of the proposed CP in Idle mode with a general transient waveform shown. The Idle mode is always characterized by the Up and Down error signals being low (i.e. Up=Down=logic 0). There are two different times in which the Idle mode occurs in the PLL control loop, each with a specific purpose: 1) during phase lock to hold the V_C value constant (i.e. ϕ_{FB} equals ϕ_{REF}) and 2) for the recharging of the capacitor, C_P, in between Pump Up and Pump Down modes (i.e., ϕ_{FB} does not equal ϕ_{REF}).

At the start of the Idle mode, switches S_1 and S_2 are closed while S_3 and S_4 are open; meanwhile this action causes C_P, to charge to V_{DD}. After C_P charges to the supply voltage, V_{DD}, the capacitor C_P holds its charge, Q_P, in an open loop fashion until the CP is instructed by the PFD to change modes to either Pump Up or Pump Down. V_C, will not change during Idle mode and, therefore, retains the voltage value, V_{C0}, it held at the moment prior to starting Idle mode, namely:

$$V_C = V_{C0}. \tag{1}$$

Due to the switched capacitor structure of the CP circuit, there are relatively little to no errors in the V_C value, ultimately reducing unwanted PLL phase errors compared to the state of the art CP designs. There is no static power being dissipated due to biasing in the proposed CP (i.e. there no current mirrors) and we must look at the switching dynamic power to find the total power consumed while the CP sits quietly in the Idle mode. In order to do this, the energy at the start and end of the Idle mode needs to be analyzed. The energy utilized by the proposed CP at the start of the Idle mode when C_P charges to V_{DD} is:

$$E_{CP_{IDLE0}} = C_P {V_{DD}}^2 = Q_P V_{DD}. \tag{2}$$

It must be noted that the CP charges only once at the very beginning of the Idle mode; this could be a full recharging or a partial recharging in (2) depending on the amount of charge

required to bring the voltage across C_P, V_P, to V_{DD}. The energy consumed by the proposed CP during the Idle mode after charging to V_{DD} is:

$$E_{CP\,\mathrm{IDLE1}} \cong 0 \tag{3}$$

due to no changes in the switches of the CP with the reasonable assumption that the leakage current flowing through the stacked switches is negligible. Therefore, the total power dissipation of the proposed CP for a complete Idle mode cycle may be found via the dynamic power equation:

$$P_{\mathrm{CP}IDLE} = \alpha f_{REF} \Delta E_{CP\,\mathrm{IDLE}} = \alpha f_{REF}(E_{CP_{IDLE0}} - E_{CP_{IDLE1}}) \tag{4}$$
$$\approx \alpha f_{REF} Q_P V_{DD}$$

where α is the activity factor ($0 \le \alpha \le 1$) for the proposed CP working in one or more specific modes at the PLL reference frequency.

3.1.2 Pump Up mode

Fig. 7 depicts the Pump Up mode for the proposed CP with a general transient waveform example. In this case, the Pump Up mode is activated by a lagging phase difference between ϕ_{FB} and ϕ_{REF}; this causes the PFD to produce a logic 1 Up error signal for the duration of the phase difference between f_{FB} and f_{REF}. The CP responds by transitioning out of Idle mode with an opening of S_2 and closing of S_4 which allows the charge, Q_P, stored on C_P to transfer to C_L, thus raising the voltage on V_C. The result for one Pump Up cycle is an increasing of ϕ_{VCO} and ϕ_{FB} in order to match ϕ_{REF}. At the end of every Pump Up cycle the CP returns to Idle mode to fully recharge C_P. As the PLL approaches phase lock, partial Pump Up cycles take place incrementally raising V_C which allows for accuracy in obtaining the desired frequency for the VCO.

The exponential capacitive behavior of the CP output, V_C, for a single Pump Up charge sharing event may be modeled by the following first order equation:

$$V_C = V_{C0} + \frac{C_P}{C_P + C_L} V_{DD}\left(1 - e^{-t/\tau_{UP}}\right) \tag{5}$$

where τ_{UP} is equal to the RC time constant for the S_1-C_P-S_4 path, $\tau_{UP} = R_{UP}Cp$, which the charge must flow through to arrive at C_L in the Pump Up mode, given that the switches, S_1 and S_4 are fully on transistors with associated resistances, R_{S1} and R_{S4}, which total to R_{UP}. The time, t, is the exact time in which the Up pulse is high, whether a partial or full cycle. If desired, the current in the Pump Up cycle can also be calculated via Ohm's law and simplified to:

$$i_C = \frac{1}{R_{UP}} \frac{C_P}{C_P + C_L} V_{DD}\left(e^{-t/\tau_{UP}}\right). \tag{6}$$

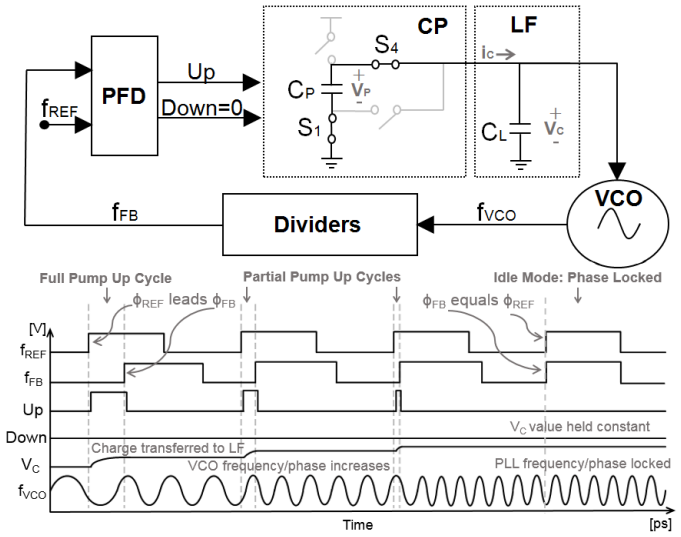

Fig. 7 Pump Up mode for the proposed PLL charge pump

As the PLL gets close to acquiring phase lock, a partial Pump Up cycle occurs where the charge transfer event will get cut off midway ($t << \tau_{UP}$) and the exponential portion of Eq. (6) may be linearly approximated to ($1\text{-}t/\tau_{UP}$) as is shown in Eq. (7) when the PLL is near phase lock:

$$\begin{aligned} V_C &\approx V_{C0} + \frac{C_P}{C_P + C_L} V_{DD}\left(1 - \left(1 - {}^{t}/_{\tau_{UP}}\right)\right) \\ &= V_{C0} + \frac{C_P}{C_P + C_L} V_{DD}\left({}^{t}/_{\tau_{UP}}\right). \end{aligned} \tag{7}$$

This linearized equation in (7) results is precise phase lock at a high resolution for the proposed charge pump and it is similar to a state of the art CP. The output step size is simply based on the ratio of C_P to the LF's C_L, when not operating at the rails. For example, to increase the output step size, increasing C_P would suffice, but further analysis on how this effects stability must be examined, which will be done in the next section. The change in energy of the charge pump system during a Pump Up mode charge sharing event is:

$$\begin{aligned} \Delta E_{CP_{UP}} &= E_{CP_{UPO}} - E_{CP_{UP1}} \\ &= \frac{1}{2} Q_P V_{DD} + \frac{1}{2} Q_L V_{C0} - \frac{1}{2} \frac{(Q_P + Q_L)^2}{C_P + C_L} \end{aligned} \tag{8}$$

where Q_P and Q_L are the initial charges held by C_P and C_L at the start of the Pump Up mode. Using Eq. (8), we can now calculate the power dissipated for the Pump Up cycle at the PLL reference frequency by using the following dynamic power equation:

$$\begin{aligned} P_{\mathrm{CP_{UP}}} &= \alpha f_{REF} \Delta E_{CP_{UP}} \\ &= \alpha f_{REF} \left(\frac{1}{2} Q_P V_{DD} + \frac{1}{2} Q_L V_{C0} - \frac{1}{2} \frac{(Q_P + Q_L)^2}{C_P + C_L}\right). \end{aligned} \tag{9}$$

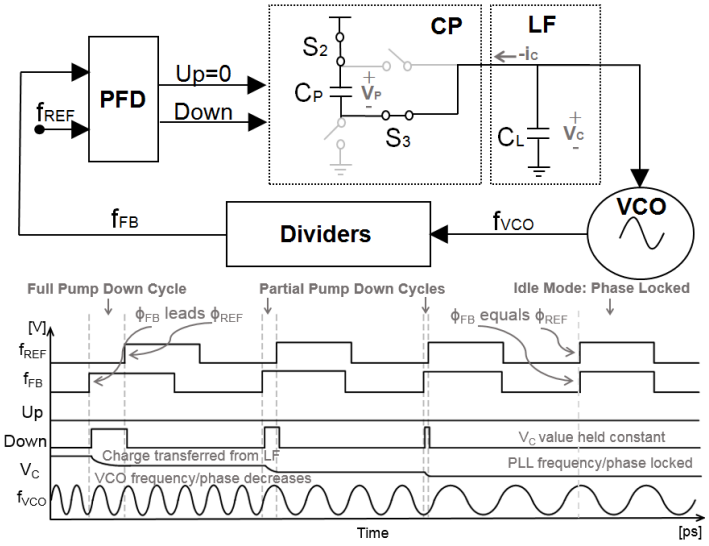

Fig. 8 Pump Down mode for the proposed PLL charge pump

3.1.3 Pump Down mode

Fig. 8 illustrates the Pump Down mode for the proposed CP with a simple transient waveform example. The Pump Down mode occurs when the phase error swings in the opposite direction and ϕ_{FB} leads ϕ_{REF}, causing the PFD to produce a logic 1 Down error signal for the duration of the difference between f_{FB} and f_{REF}. Similar to the Pump Up mode, the CP responds by moving out of the Idle mode, but instead opens S_1 and closes S_3 which allows the pulling of the stored charge, Q_P, away from C_L, thus lowering the voltage on V_C. This action decreases f_{VCO} and, consequently, f_{FB}, in the closed PLL control loop. At the end of every Pump Down cycle, the CP recharges C_P in the Idle mode.

Analogous to the Pump Up cycle, the Pump Down CP output can be modeled by the first order equation:

$$V_C = V_{C0} - \frac{C_P}{C_P + C_L} V_{DD}\left(1 - e^{-t/\tau_{DN}}\right) \tag{10}$$

where τ_{DN} is equal to the RC time constant for the S_3-C_P-S_2 path, $\tau_{DN} = R_{DN}Cp$, which the charge must flow through to leave C_L in the Pump Down mode. Similar to Eq. (5), the switches S_3 and S_2 are transistors fully on with associated resistances, R_{S3} and R_{S2}, which total to R_{DN}. The time, t, is the full or partial cycle time that the Down error signal is high. If desired, the current in the Pump Down cycle can also be calculated such as was done in Eq. (6), with the noted polarity difference:

$$-i_C = -\frac{1}{R_{DN}} \frac{C_P}{C_P + C_L} V_{DD}\left(e^{-t/\tau_{DN}}\right). \tag{11}$$

As the PLL draws near to phase lock, partial Pump Down cycles occur, where the charge transfer event will get cut off midway ($t << \tau_{DN}$). In this case Eq. (11) may be linearly approximated to:

$$\begin{aligned} V_C &\approx V_{C0} - \frac{C_P}{C_P + C_L} V_{DD}\left(1 - \left(1 - {}^{t}/_{\tau_{DN}}\right)\right) \\ &= V_{C0} - \frac{C_P}{C_P + C_L} V_{DD}\left({}^{t}/_{\tau_{DN}}\right). \end{aligned} \tag{12}$$

The output Down step size of the CP may be adjusted via the ratio of C_P to the LF's C_L and is equivalent to the Up step size due to C_P being utilized for both transitions, thus eliminating the need for extra matching circuitry compared to the state of the art. The CP's energy used during a Pump Down cycle is:

$$\begin{aligned} \Delta E_{CP\,DN} &= E_{CP_{DNO}} - E_{CP\,DN1} \\ &= \frac{1}{2}\frac{C_P}{C_P + C_L} Q_P V_{DD} + \frac{1}{2} Q_L V_{C0}. \end{aligned} \tag{13}$$

Finally, the power dissipated for the Pump Down mode is:

$$\begin{aligned} P_{\mathrm{CP_{DN}}} &= \alpha f_{REF} \Delta E_{CP_{DN}} \\ &= \alpha f_{REF}\left(\frac{1}{2}\frac{C_P}{C_P + C_L} Q_P V_{DD} + \frac{1}{2} Q_L V_{C0}\right). \end{aligned} \tag{14}$$

3.2 Total power consumption

The total dynamic power of the proposed CP may be found by adding (4), (9), and (14) or via the C_P's stored energy over time:

$$\begin{aligned} P_{CP_{dyn}} &= P_{CP_{IDLE}} + P_{CP_{UP}} + P_{CP_{DOWN}} \\ &\cong \left(\alpha f_{REF} \frac{C_P {V_{DD}}^2}{2}\right) = \left(\alpha f_{REF} \frac{Q_P V_{DD}}{2}\right). \end{aligned} \tag{15}$$

Therefore, the total power of the proposed CP with negligible leakage of the stacked transistor switches is simply:

$$\begin{aligned} P_{CP} &= P_{CP_{dyn}} + P_{CP_{leak}} \\ &= \left(\alpha f_{REF} \frac{C_P {V_{DD}}^2}{2}\right) + (I_{leak} V_{DD}) \\ &\cong \alpha f_{REF} E_{CP}\ . \end{aligned} \tag{16}$$

3.4 Stability analysis

A typical charge-pump PLL of the type shown in Fig. 1 can be modeled as a linear system shown in Fig. 9, as long as the PLL loop bandwidth, f_c, is much less than the reference frequency (e.g. $f_c = (1/10)\ f_{REF}$) [2, 6-8]. The reason this PLL demands a small f_c is to maintain stability of the CPPLL due to its inherent sample and hold nature. In Fig. 9, the gain of the phase frequency detector is K_p. For a PLL in the process of acquiring phase lock which utilizes the proposed CP, $Kp = i_c/2\pi$, where i_c is the proposed CP current which can be found by Eq. (6) for the Pump Up mode or Eq. (11) for the Pump Down mode. Also shown in Fig. 9, the loop filter is modeled with the impedance, Z(s), the VCO is modeled as an integrator with a gain of K_{VCO}, and the divider by 1/M, where M is the division factor.

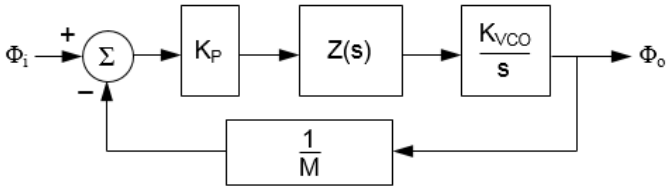

Fig. 9 General linearized model of a charge pump PLL [2, 6-7]

The closed loop gain, A_{CL}, of the linearized PLL model in Fig. 9 is [2, 6-8]:

$$A_{CL} = \frac{\phi_o(s)}{\phi_i(s)} = \frac{G(s)}{1 + G(s)H(s)} = \frac{G(s)}{1 - LT}, \tag{17}$$

where the forward gain is:

$$G(s) = \frac{K_P K_{VCO} Z(s)}{s} = \frac{i_C K_{VCO} Z(s)}{2\pi s}, \tag{18}$$

the feedback division factor is:

$$H(s) = \frac{1}{M}, \tag{19}$$

and loop transmission, LT, can be found by:

$$LT = -G(s)H(s) = -\frac{K_P K_{VCO} Z(s)}{Ms} = -\frac{i_C K_{VCO} Z(s)}{2\pi M s}. \tag{20}$$

The order of a PLL is generally given by the number of poles contributed by Z(s) and the single pole contribution of the VCO. The order of the PLL is important to understand the characteristics of the PLL and the tradeoffs between stability, settling time, noise, and additional area if the components of the LF are increased. For example, a 3rd order PLL typically will have more spurious tone suppression, but it can have extra phase lag which if not carefully designed can have stability issues [6].

The next step in analyzing the stability of the PLL is to investigate the realization of the loop filter circuit and to find its impedance, Z(s). The proposed charge pump is unlike the traditional designs, in that it includes a capacitor, C_P, along with minimally-sized switches which can be modeled as resistors. Therefore, the model of the proposed CP with its capacitor and resistors have a contribution to Z(s) that must be taken into account to understand the stability of the PLL. By inspection, due to there being two capacitors, C_P and C_L, in Fig. 4, it can be deduced that the CP-LF combination results in two poles which contribute the order of the PLL, in this case, a 3rd order PLL overall.

Another way to look at this, is to observe the CP-LF combination when the PLL has not yet acquired phase lock such as when the CP is operating in the Pump Up or Pump Down modes as shown in Fig. 10. Fig. 10 shows examples of the charge pump voltage output, V_C, for (a) a state of the art CP and (b) the proposed CP output. For example, in the Pump Up mode, each V_C output pulse of the state of the art CP is like a

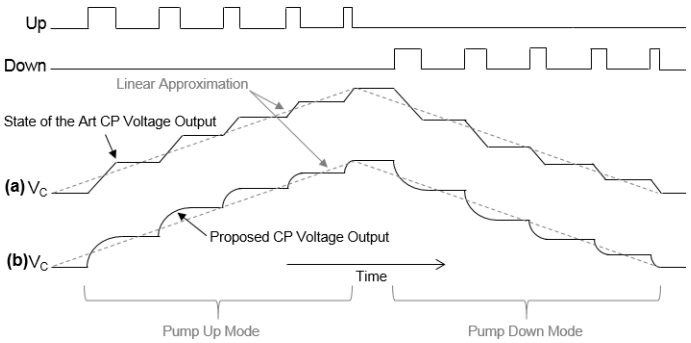

Fig. 10 General time domain CP voltage output ramp function linearized appoximation of (a) a state of the art CP and (b) the proposed CP for the Pump Up and Pump Down modes

linear ramp in the time domain, which can be converted via Laplace to:

$$f(t) = t \leftrightarrow F(s) = \frac{1}{s^2}. \tag{21}$$

Noting that Eq. (21) has a two pole contribution to the PLL. On the other hand, the proposed CP has exponential steps described by Eq. (5) for the Pump Up mode in the time domain which can be converted via Laplace by:

$$f(t) = e^{-at} \leftrightarrow F(s) = \frac{1}{s + a}. \tag{22}$$

This time noting that in each full step of the Pump Up mode there is a one pole contribution to the PLL when not in phase lock.

As the PLL with the proposed CP nears phase lock in the Pump Up mode, partial pump up cycles occur and we can use Eq. (7) to approximate a linearized time-based response, thus allowing use to use Eq. (20) to convert to the frequency domain. This is also true if we look at the linear approximations of the ramp-like time domain functions of Fig. 10 (a) and (b) over many cycles, where we can again use Eq. (20) to estimate a two pole contribution from the CP-LF combination to the PLL by both the state of the art and proposed CPs while operating. A similar investigation can be done using the Pump Down mode with Eqs. (10) and (12). This gives us insight in to how to model the proposed CP with the LF.

To model the proposed CP in a PLL, we take the approach of carefully examining the circuit realization for the combination of the proposed CP with the LF as shown in Fig. 11 (a). Simplified versions of the CP-LF combination modeled in the Pump Up mode from Fig. 7 and the Pump Down mode in Fig. 8 are shown in Fig. 11 (b) and (c), respectively.

For example, we will proceed by analyzing the Pump Up mode circuit model in Fig. 11 (b). In Pump Up mode, the switch resistances R_{S2} and R_{S3} are assumed to be large, approaching infinity, therefore they are modelled ideally as open, for the sake of analysis. In the same circuit, switches S_1 and S_4 are modeled with the resistances, R_{S1} and R_{S4}. The reusable charge pump capacitor, C_P, and the simple loop filter capacitor, C_L, combine to make a 2nd order filter, which contributes to a 3rd order PLL.

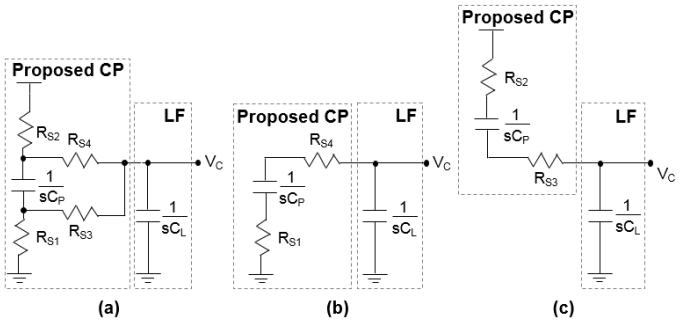

Fig. 11 Basic impedance circuit model for (a) the combination of the proposed CP with the LF, and the equivalent circuit models for the (b) the Pump Up and (c) the Pump Down modes

A similar diagram and analysis can be performed with the CP operating in Pump Down mode while the PLL is in the process of acquiring phase lock. The equivalent circuit is shown in Fig. 11 (c). Ideally, we want R_{S1}=R_{S2} and R_{S4}=R_{S3} when any of these switches are closed during their respective operating modes. As previously mentioned, when not in use, we want the resistance of any of the open switches to be very large, as to model an open circuit for the switch.

Using Fig. 11 (b) for the Pump Up case, the impedance of the 2nd order CP-LF combination is:

$$Z(s) = \frac{\tau_1 s + 1}{sC_P\left(1 + \frac{C_L}{C_P}\right)[A(\tau_1 s) + 1]}, \tag{23}$$

where

$$A = \frac{1 + b\frac{\tau_2}{\tau_1}}{1 + b} \approx \frac{1}{1 + b},$$

$$\tau_1 = R_{S1}C_P\,, \qquad \tau_2 = R_{S4}C_L\,, \qquad b = \frac{C_P}{C_L}.$$

The phase margin, PM, is calculated to be [6-8]:

$$PM = tan^{-1}(\tau_1\omega_C) - tan^{-1}A(\tau_1\omega_C)\,. \tag{24}$$

If we approximate A as shown above, we can find the crossover frequency, ω_C, to be:

$$\omega_C \approx \frac{\sqrt{1+b}}{\tau_1}\,, \tag{25}$$

Which allows the phase margin to be simplified to:

$$PM \approx tan^{-1}\sqrt{1+b} - tan^{-1}\frac{1}{\sqrt{1+b}}, \tag{26}$$

With this approximated information we can now pick an appropriate ratio for the C_P to C_L capacitors in the proposed CP for a phase margin that delivers the lowest settling time, while maintaining stability in the PLL. Fig. 12 depicts the simulated results when the phase margin is plotted while varying the ratio between the loop filter and charge pump capacitors. Evaluating the settling time of a 3rd order PLL versus the phase margin was done by simulation as shown in Fig. 13. From Fig. 13, it can be seen that the lowest settling time takes place when the phase margin is approximately 50°. In Fig. 12, a phase margin of 50° corresponds to a loop filter to charge pump capacitor ratio of 10. For example, in an integrated circuit, C_L could be chosen to be 1pF, and C_P to be 100fF, resulting in the ratio of 10. Additionally, a ratio of $\tau_1/\tau_2 = 0.05$ can be achieved by the appropriate sizing of the transistor switches for the given C_L/C_P ratio of 10.

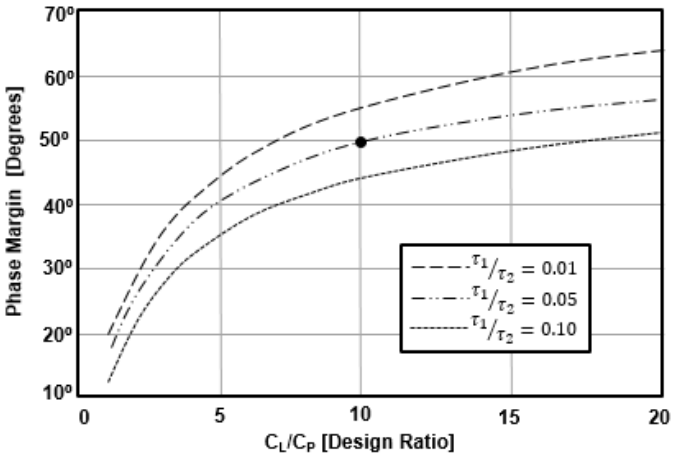

Fig. 12 Simulated maximum phase margin as a funtion of C_L/C_P capacitor ratios in a 3rd order PLL

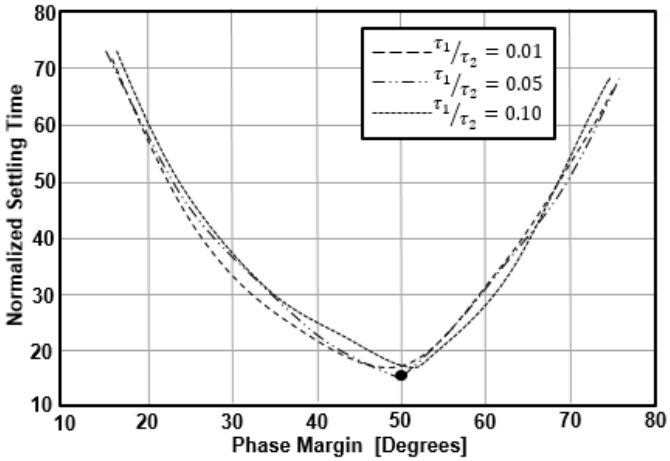

Fig. 13 Simulated normalized settling time as a function of phase margin in a 3rd order PLL

3.5 Noise contribution

There are several sources of noise in the charge pump PLL, as shown in Fig. 14, including the VCO noise, φ_{nv}, and the noise of the reference signal, φ_{ni}. Additionally, the noise from the PFD, CP, LF, and dividers can all be included in φ_{ni}. Using the linearized model of the PLL with reference noise added in Fig. 14, the noise transfer function from input to output phase transfer function can be found by:

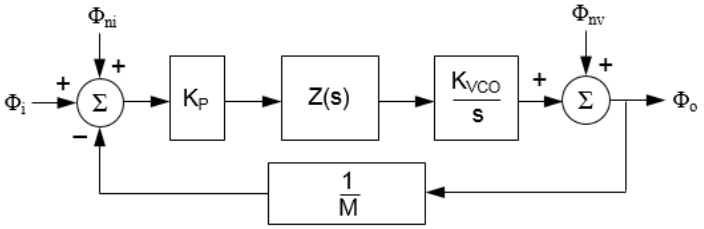

Fig. 14 Linearized noise model for the charge pump PLL with noise added at the input and output [6, 8]

$$\frac{\varphi_o(s)}{\varphi_{ni}(s)} = \frac{K_P K_{VCO} N(s)}{sD(s) + \frac{K_P K_{VCO}}{M} N(s)}, \tag{27}$$

where N(s) and D(s) are the numerator and denominator of the loop filter transfer function. The only source of noise in the CP-LF combination are the switch resistors. For example, in the Pump Up mode these are R_{S1} and R_{S4} as shown in Fig. 11 (b). The transfer function from the equivalent voltage noise of R_{S1}, V_{N1}^2, to the output can be calculated by:

$$\frac{\varphi_o}{V_{n1}} = \frac{sC_P}{R_{S1}C_P s + 1}\left(\frac{\varphi_o(s)}{\varphi_{ni}(s)}\right), \tag{28}$$

where:

$$\overline{V_{n1}^{\,2}} = 4KTR_{S1}\Delta f. \tag{29}$$

Similarly,

$$\frac{\varphi_o}{V_{n4}} = \left(1 + \frac{C_L}{C_P} + R_{S4}C_L s\right)\frac{sC_P}{R_{S1}C_p s + 1}\left(\frac{\varphi_o(s)}{\varphi_{ni}(s)}\right), \tag{30}$$

where:

$$\overline{V_{n4}^{\,2}} = 4KTR_{S4}\Delta f. \tag{31}$$

It must be noted that due to the additional zeros in Eqs. (28) and (30) as compared to Eq. (27), the output noise due to the thermal noise of the switch resistors will first increase, then decrease. Therefore, the designer must verify that the thermal noise which due to these switches is acceptable in order to minimize noise peaking at low frequencies and maintain low noise at higher frequencies. A similar noise analysis can be done for the Pump Down mode by allowing the ideal case that R_{S1}=R_{S2} and R_{S4}=R_{S3}.

3.6 Output mismatch analysis

Now that we have an idea of how to appropriately size the transistors and capacitors for the CP and LF in a PLL for stability and desired step size, we can proceed to analyze the symmetry or mismatch between the voltage outputs from the Pump Up and Pump Down modes. Fig. 15 is an example of the simulated output for the proposed CP with a C_P to C_L ratio of 100fF to 1pF. In this plot, it can be seen that the outputs for the Pump Up mode are equivalent to the size for the Pump Down mode as desired.

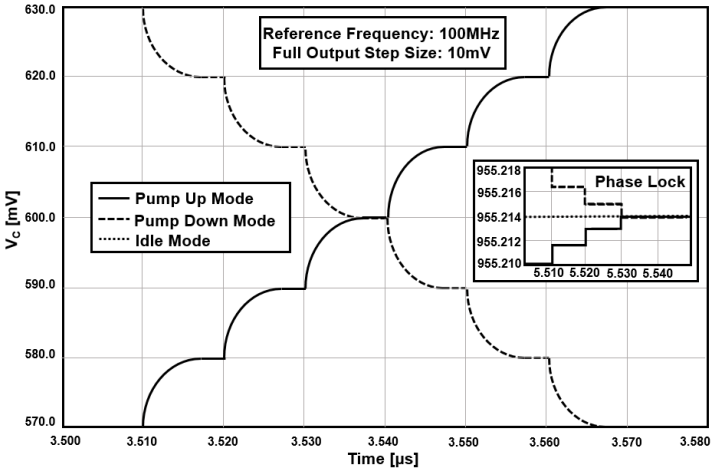

Fig. 15 Simulated plot of the proposed CP output step and phase lock behavior

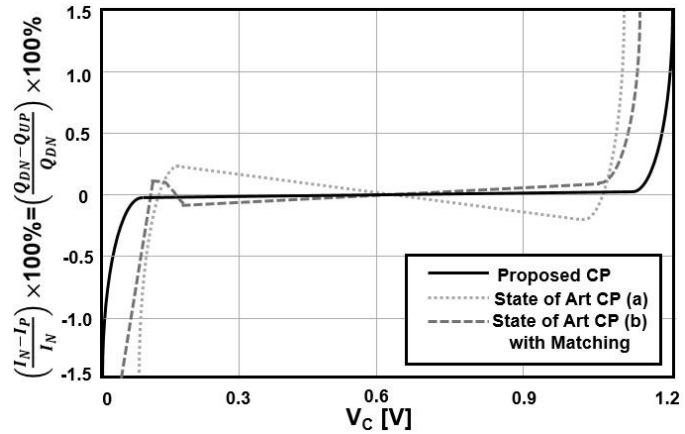

Fig. 16 Simulated systematic % error between Up and Down currents as a function of V_C of proposed CP and state of the art CPs from Fig. 3 (a) and (b)

Fig. 16 goes one step further to examine the simulated systematic % error between the Pump Up and Pump Down currents as a function of the control voltage output of the CP. In this diagram, we have also simulated the state of the art charge pumps from Fig. 3 (a) and (b) as to get a sense of the accuracy of the proposed CP design. Notably, the proposed CP output has less than a 0.05% error for $0.05V \leq V_C \leq 1.15V$.

4 Implementing the proposed CP in a multi-GHz PLL

The ultimate goal for inventing this novel charge transfer-based CP is to implement it in an all-digital CMOS, multi-GHz PLL. Doing so will allow for a low power, high performance analog CPPLL that has the ability to scale to the newest process nodes. This section briefly highlights the proposed CPPLL blocks employed to showcase the proposed CP design. Although the proposed CPPLL blocks shown are not required to be used with the proposed CP, we will highlight any design considerations, beyond the previous analysis or the CP-LF combination, that should be observed to make a quality analog frequency synthesizer in a digital nanoscale process. Fig. 17 displays an overview of the blocks in the proposed CPPLL.

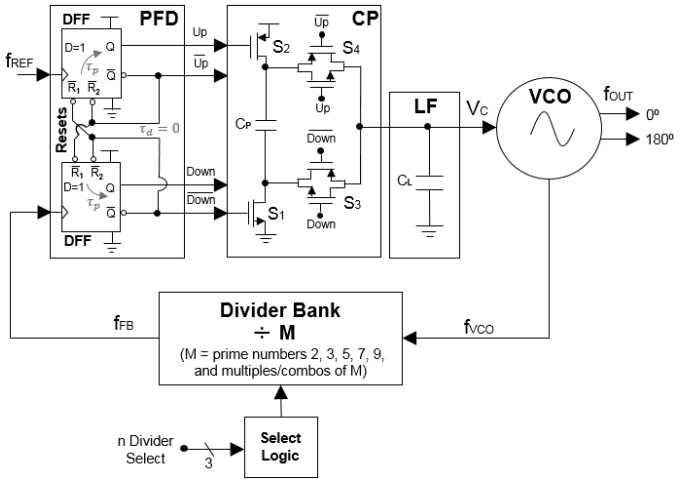

Fig. 17 Proposed CPPLL implementation

4.1 No-added delay phase-frequency detector

Out of all of the blocks in the CPPLL, the PFD is the block that will actually need some altering to accommodate the proposed CP. Namely, the proposed CP does not need the extra-added delay stage in the state of the art PFDs shown in Fig. 18 (b) that is required to slow down the switching speed of the PFD to match the large analog switches in state of the art CPs. For instance, if the error pulse width of the PFD becomes too narrow as the PLL approaches phase lock, the state of the art CP switches will not be able to respond to a PFD with no-added delay, thus creating an unwanted dead band of how close the PLL can get to phase lock. On the other hand, if too much delay is added, it causes the state of the art CP to overshoot by some amount, causing an undesirable dithering of the VCO frequency around phase lock.

The proposed CP employs minimally-sized digital-like transistors as switches that have the ability to switch at the same speed of the D-flip flops (DFFs) inside of the PFD, such that:

$$\tau_{p_{up}} = \tau_{p_{dn}} = \tau_{S_1} = \tau_{S_2} = \tau_{S_3} = \tau_{S_4} . \quad (32)$$

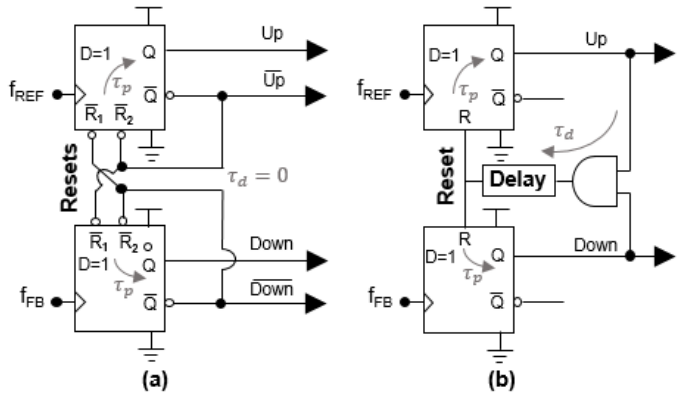

Fig. 18 (a) The proposed PFD with no-added delay and (b) a traditional PFD with added delay in the feedback path

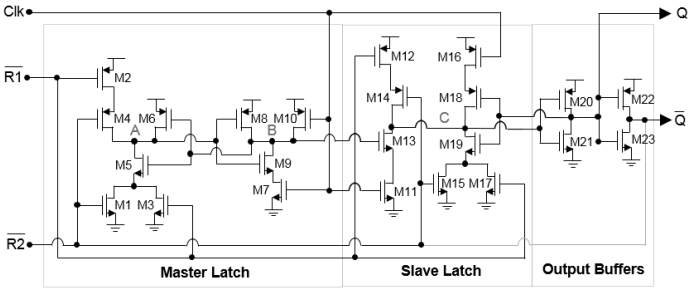

Fig. 19 The proposed PFD DFF, where D=1 and $\bar{Q}$=$\bar{R}_2$ for no-added delay

Therefore, no-added delay is required in the PFD as shown in Fig. 18 (a) [10]. This results in a smaller area and a lower power for the PFD and precise phase lock in the proposed CPPLL.

An example of a high-speed DFF which uses a method called complex complementary logic (C^2L) for maximal optimization of speed, power, and area is shown in Fig. 19 [11]. If it was desired to utilize this DFF in a PFD with a state of the art CP, the required delay in the form of buffers could be added between the $\bar{Q}$ and $\overline{R_2}$ nodes in Fig. 19.

4.2 Capacitively-coupled VCO

For the scalable, multi-GHz VCO, a capacitively-coupled oscillator which uses current-bypass inverter stages as shown in Fig. 20 was designed for the proposed CPPLL [12]. In this novel VCO, charge is recycled between the nodes connecting the capacitors, making a continual inductor-like loop through the branches, resulting in a high-spectral purity ring oscillator that can be fabricated in nanoscale CMOS processes. By increasing V_C, from 0V to V_{DD}, the tuning of the capacitors is altered and current starved from the inverter, thereby decreasing the frequency. For instance, if V_C=0V, the maximum output frequency can be noted for the VCO. The output frequency of the VCO can be found by the equation:

$$f_{OUT} = \frac{1}{\tau_{total}} = \frac{1}{\tau_{ring}+\tau_{interconnect}} = \frac{1}{(2s\tau_{pd}) + (2(r-1)R_{eq}C_{eq})} \quad (33)$$

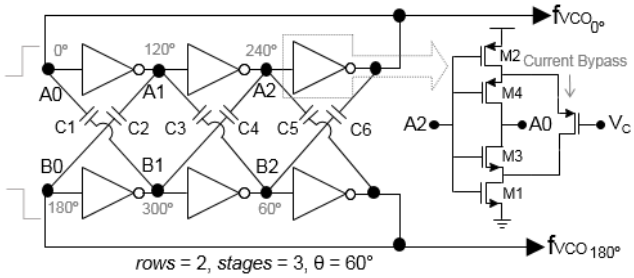

Fig. 20 The proposed VCO with voltage-controlled current bypass inverter stages

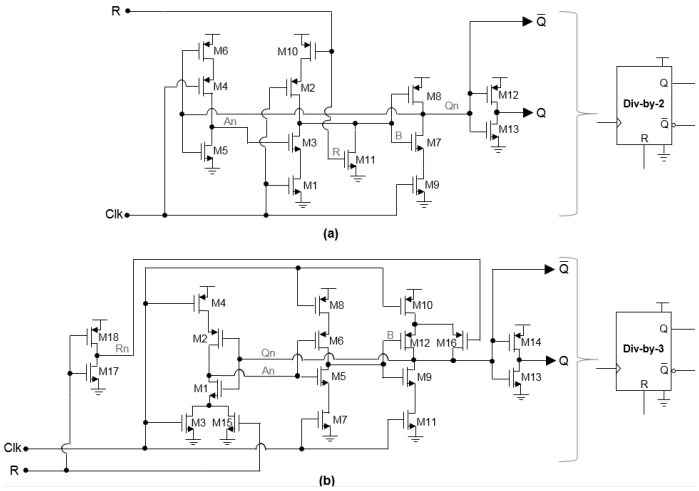

Fig. 21 Examples of the proposed dynamic prime number dividers including (a) divide-by-2 and (b) divide-by-3

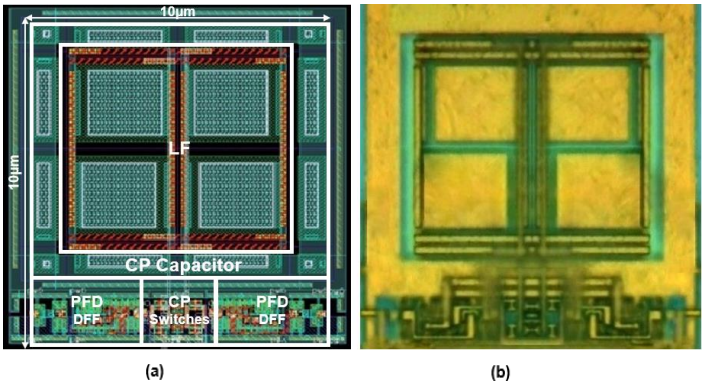

Fig. 22 The proposed PLL charge pump (a) layout and (b) die micrograph

where r is the number of rows of the VCO, s is the number of stages, R_{eq} and C_{eq} is the equivalent resistance and capacitance, respectively, seen at the node that f_{OUT} is being taken from.

4.3 Dynamic prime number dividers

For the divider block, dynamic prime-number dividers (e.g. M=2, 3, 5, 7, and 9) and their combinations/multiples were placed in a divider bank controlled by select logic. For example, if a divide integer of M=50 is desired, the prime number divider combination of 5, 5, and 2, with be selected. The designs of the dynamic prime number dividers were again designed with the C^2L methodology in [11]. Fig. 21 (a) and (b) show the divide-by-2 and divide-by-3 digital circuits. The dynamic prime number divider circuits are all designed with digital devices and scalable.

5 Experimental results

This section presents the post-silicon measurement results for the proposed work including the proposed CP and its implementation in the proposed 0.5-10GHz CPPLL. The proposed CP and CPPLL were fabricated in was a TSMC all-digital 40nm CMOS process. The six transistors of the CP had a width of W_N=120nm or W_P=240nm and a length of L=40nm. The CP capacitor, C_P, was 100fF, while the LF capacitance, C_L, was 1pF, resulting in both stability and a 1:10 output step size ratio. The PFD utilized was a dual-reset DFF with no added delay due to the comparable switching time between the minimally-sized switches of the PFD DFFs and the CP. The VCO utilized was a differential capacitively-coupled ring oscillator with a tuning range from 0.5-10GHz. Dynamic prime number dividers controlled by select logic were also utilized.

Fig. 22 depicts the layout and die micrograph of the fabricated proposed CP in the PLL.

Table 1 Silicon measurements and performance summary of the proposed charge pump with a comparison to state of the art charge pumps used in PLLs

	This work	**(a)[a]**	**(b)[a]**	**[3]**	**[4]**	**[5]**
Supply [V]	0.2-1.2	1.2	1.2	3.3	1.8	1.5
f_{VCO} [GHz]	0.5-10.0	1-10	1-10	0.35-0.61	--	4.8-5
f_{REF} [MHz]	50-1000	50-400	50-400	20	50-500	11
CP power [W]	250p	1.12m	1.53m	1.5m[b]	940µ	2.2m
V_C [V]	0.0-1.2	0.1-1.1	0.1-1.1	0.07-1.05	0.1-0.9	0.1-1.4
CP area [mm^2]	0.0004	0.0045	0.0065	0.015	0.015	0.16
RMS jitter [ps]	0.80± 0.05	2.3	1.5	7.1	--	--
Ref. spurs [dBc]	<-70	<-60	<-65	--	--	<-70
Phase error [°]	0.1-0.3	2.3	0.9	--	1-5	--
CMOS technology	40nm	40nm	40nm	0.35µm	0.18µm	0.24µm

[a] Simulated results from state of the art CP examples in Fig. 3 (a) and (b)

[b] Estimated value

Experimental results of the proposed CP are shown in Table 1. For comparison, simulation results of the state of the art CPs shown in Fig. 3 (a) and (b) along with post-silicon measurements of other reported state of the art CPs are illustrated next to the fabricated CP results. Results for the proposed CP were taken at f_{VCO}=5GHz and f_{REF}=100MHz with a 1.2V supply and a divider of M=50. The average power of the CP was 250pW, while (a) and (b) had a static power of 1.12mW and 1.53mW, respectively, resulting in a 10^6 improvement in power consumption over the state of the art. Also notable, is the proposed CP's compact area and ability to be utilized at low supply voltages when compared to the state of the art CP designs.

Table 2 Silicon measurements and performance summary of the proposed CPPLL and a comparison to state of the art PLLs

	This work	[13]	[14]	[15]	[16]	[17]
PLL type	Analog CPPLL	Analog CPPLL	Analog CPPLL	Digital	Digital	Hybrid
Frequency [GHz]	0.5-10.0	1.0-8.5	0.5-2.5	0.6-0.8	0.39-1.41	1.4-3.2
Reference [MHz]	50-400	50-450	10-100	2-40	40-350	36-108
VCO freq. [GHz]	5.0	2.5	1.0	0.8	0.9	3.1
Clock ref. [MHz]	100	100	100	26	150	108
RMS jitter [ps]	0.80±0.05	0.99	2.36	20-30	1.7	1.01
Power [mW]	0.80	70.0	25.0	2.66	0.78	27.5
Supply [V]	1.2	2.5	1.8	1.2	0.8	1.2
Area [mm^2]	0.0040	0.277	0.15	0.027	0.0066	0.32
CMOS technology	40nm	45nm SOI	0.18µm	65nm	65nm	65nm

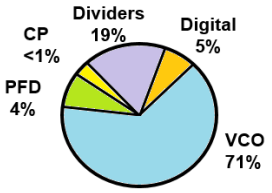

Fig. 23 Breakdown of the power consumption for the proposed CPPLL between its constitute blocks

Results of the overall proposed CPPLL implementation are shown in Table 2. Fig. 23 depicts the power usage of the various blocks in the proposed CPPLL, with the proposed CP taking up less than 1% of the overall power. Fig. 24 illustrates a snapshot of the phase noise and spectrum characteristics of the physically tested PLL with the proposed CP. The unique, low power switched capacitor design of the proposed CP is responsible for the desirable minimal charge injection into the VCO control line. The power of the spurious sidebands of the PLL thereby is greatly reduced allowing for the reference spurs to be less than -70dBc.

6 Conclusion

The proposed CP design overcomes traditional design concerns efficiently by eliminating current mirrors and adopting a switched capacitor approach to transferring charge to and from the LF's capacitance incrementally when the PLL is in the process of acquiring phase lock. Once in phase lock, the proposed CP has extremely low leakage, allowing the VCO to operate undisturbed. Additionally, the proposed CP switches at

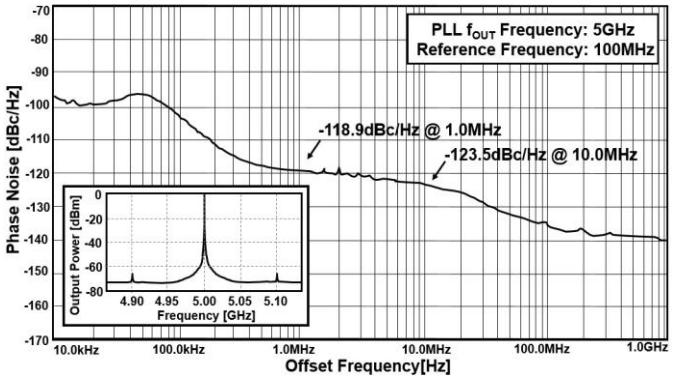

Fig. 24 Snapshot of the silicon measurements of the PLL phase noise and spectrum characteristics

the same speed of the DFFs within the PFD, therefore no extra delay is required between the PFD and CP blocks, as is the norm for state of the art approaches. The result is a dramatic reduction of power and active area in both the CP and overall PLL. Furthermore, the proposed CP is scalable to and between nanoscale CMOS process nodes and able to be used at very low voltages (<1V) as it is not limited by transistor threshold stacking. The proposed CP possesses no analog process extensions that are parametrically sensitive to process variation, allowing for a symmetrically matched Up and Down output voltage step when the PLL is in the process of acquiring phase lock, because the same capacitor is reconfigured for reuse to transfer charge to and from the loop filter. Finally, the use of the proposed CP allows for a low jitter, low phase-noise analog PLL with reduced reference spurs.

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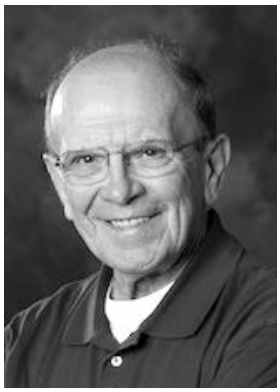

John Choma, Jr. earned his B.S., M.S., and Ph.D. degrees in Electrical Engineering from the University of Pittsburgh in 1963, 1965, and 1969, respectively. He was Professor of Electrical Engineering and the former Chair of the Ming Hsieh Department of Electrical Engineering at the University of Southern California, where he taught undergraduate and graduate courses in electrical circuit theory, passive and active filters, and analog integrated electronics. Professor John Choma, Jr. is the author or co-author of some 160 journal and conference papers and multiple books, and the presenter of more than sixty-five invited short courses, seminars, and tutorials, is the 1994 recipient of the Prize Paper Award from the IEEE Microwave Theory and Techniques Society. John has served the IEEE Circuits and Systems Society as a member of its Board of Governors, its Vice President for Administration, and its President. He also served as the International Chair of the IEEE Gustav Robert Kirchhoff Awards Committee. John has been an Associate Editor and Editor-In-Chief of the IEEE Transactions on Circuits and Systems, Part II. He was an Associate Editor of the Journal of Analog Integrated Circuits and Signal Processing and a former Regional Editor of the Journal of Circuits, Systems, and Computers. A Fellow of the IEEE, Prof. Choma has been awarded the IEEE Millennium medal and has received three awards from the IEEE Circuits and Systems Society; namely, the Golden Jubilee Award, the 1999 Education Award, and the 2000 Meritorious Service Award.