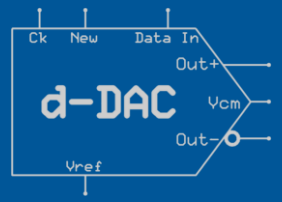
Circuit Seed™

16-Bit Recirculating Differential DAC



V_{dd}: **0.5V to 2V**

Throughput: **~1MSPS**

Resolution: **16-bits**

Conversion period: **16 µs @1MHz clock**

Amplifier SNR: **-150 dB**

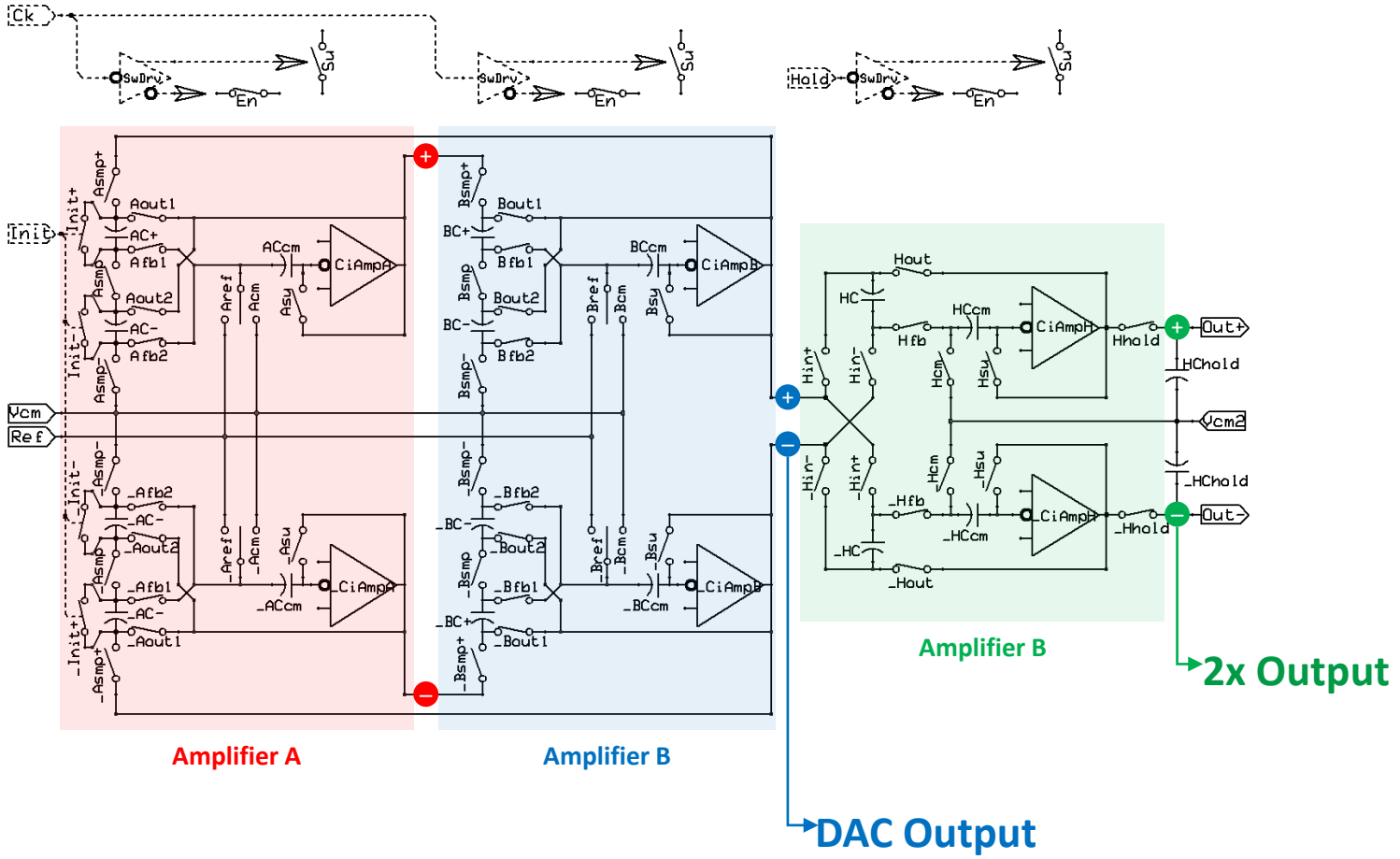
Harmonic distortion: **-150dB**

Temperature Range: **–125 °C to 250 °C**

Power consumption: **~740.65 µw @1.8V**

Energy consumption: **~11.85** $\frac{\textbf{nano-Joules}}{\textbf{conversion}}$ **@1.8V**

130nm example which scales to IC process ring oscillator rates
Works in any IC process including all-digital processes



Simulation #	Sch Name	Amplifier A: Odd Stage	Hold [mV] @19us 2x Out	DAC [mV] @ 18us DAC Out	Error [µV] @19us 2x Out	Error [µV] @ 18us DAC Out
0		**BaseLine**	**-450.947**	**-225.433**		
1	ApS1	PAmpAS1+	-450.959	-225.439	-12	-6
2	ApS2	PAmpAS2-	-450.947	-225.433	0	0
3	ApS3	PAmpASOut	-450.947	-225.433	0	0
4	_ApS3	_PAmpASOut	-450.948	-225.434	-1	-1
5	_ApS2	_PAmpAS2-	-450.947	-225.433	0	0
6	_ApS1	_PAmpAS1+	-450.935	-225.428	12	5
11	ApD1	PAmpAD1+	-450.95	-225.435	-3	-2
12	ApD2	PAmpAD2-	-450.947	-225.433	0	0
13	ApD3	PAmpADOut	-450.945	-225.432	2	1
14	_ApD3	_PAmpADOut	-450.949	-225.435	-2	-2
15	_ApD2	_PAmpAD2-	-450.947	-225.433	0	0
16	_ApD1	_PAmpAD1+	-450.945	-225.432	2	1
21	AnD1	NAmpAD1+	-450.946	-225.433	1	0
22	AnD2	NAmpAD2-	-450.947	-225.433	0	0
23	AnD3	NAmpADOut	-450.946	-225.433	1	0
24	_AnD3	_NAmpADOut	-450.948	-225.434	-1	-1
25	_AnD2	_NAmpAD2-	-450.947	-225.433	0	0
26	_AnD1	_NAmpAD1+	-450.948	-225.434	-1	-1
31	AnS1	NAmpAS1+	-450.936	-225.428	11	5
32	AnS2	NAmpAS2-	-450.947	-225.433	0	0
33	AnS3	NAmpASOut	-450.947	-225.433	0	0
34	_AnS3	_NAmpASOut	-450.947	-225.434	0	-1
35	_AnS2	_NAmpAS2-	-450.947	-225.433	0	0
36	_AnS1	_NAmpAS1+	-450.957	-225.439	-10	-6

Simulation #	Sch Name	Amplifier B: Even Stage	Hold [µV] @19us 2x Out	DAC [µV] @ 18us DAC Out	Error [µV] @19us 2x Out	Error [µV] @ 18us DAC Out
0		**BaseLine**	**-450.947**	**-225.433**		
1	BpS1	PAmpBS1+	-450.968	-225.445	-21	-12
2	BpS2	PAmpBS2-	-450.924	-225.434	23	-1
3	BpS3	PAmpBSOut	-450.955	-225.434	-8	-1
4	_BpS3	_PAmpBSOut	-450.938	-225.433	9	0
5	_BpS2	_PAmpBS2-	-450.971	-225.434	-24	-1
6	_BpS1	_PAmpBS1+	-450.927	-225.421	20	12
11	BpD1	PAmpBD1+	-450.949	-225.436	-2	-3
12	BpD2	PAmpBD2-	-450.942	-225.433	5	0
13	BpD3	PAmpBDOut	-450.942	-225.432	5	1
14	_BpD3	_PAmpBDOut	-450.952	-225.435	-5	-2
15	_BpD2	_PAmpBD2-	-450.953	-225.433	-6	0
16	_BpD1	_PAmpBD1+	-450.945	-225.431	2	2
21	BnD1	NAmpBD1+	-450.948	-225.433	-1	0
22	BnD2	NAmpBD2-	-450.949	-225.434	-2	-1
23	BnD3	NAmpBDOut	-450.947	-225.433	0	0
24	_BnD3	_NAmpBDOut	-450.947	-225.434	0	-1
25	_BnD2	_NAmpBD2-	-450.946	-225.433	1	0
26	_BnD1	_NAmpBD1+	-450.946	-225.434	1	-1
31	BnS1	NAmpBS1+	-450.928	-225.423	19	10
32	BnS2	NAmpBS2-	-450.967	-225.434	-20	-1
33	BnS3	NAmpBSOut	-450.957	-225.433	-10	0
34	_BnS3	_NAmpBSOut	-450.935	-225.434	12	-1
35	_BnS2	_NAmpBS2-	-450.927	-225.433	20	0
36	_BnS1	_NAmpBS1+	-450.967	-225.444	-20	-11

Simulation #	Sch Name	Amplifier H:	Hold [µV] @19us 2x Out	DAC [µV] @ 18us DAC Out	Error [µV] @19us 2x Out	Error [µV] @ 18us DAC Out
0		**BaseLine**	**-450.947**	**-225.433**		
1	HpS1	PAmpHS1+	-450.957	-225.434	-10	-1
2	HpS2	PAmpHS2-	-450.947	-225.433	0	0
3	HpS3	PAmpHSOut	-450.947	-225.433	0	0
4	_HpS3	_PAmpHSOut	-450.947	-225.433	0	0
5	_HpS2	_PAmpHS2-	-450.947	-225.433	0	0
6	_HpS1	_PAmpHS1+	-450.937	-225.433	10	0
11	HpD1	PAmpHD1+	-450.949	-225.433	-2	0
12	ApD2	PAmpHD2-	-450.947	-225.433	0	0
13	HpD3	PAmpHDOut	-450.945	-225.433	2	0
14	_HpD3	_PAmpHDOut	-450.950	-225.433	-3	0
15	_HpD2	_PAmpHD2-	-450.947	-225.433	0	0
16	_HpD1	_PAmpHD1+	-450.945	-225.433	2	0
21	HnD1	NAmpHD1+	-450.947	-225.433	0	0
22	HnD2	NAmpHD2-	-450.947	-225.433	0	0
23	HnD3	NAmpHDOut	-450.946	-225.433	1	0
24	_HnD3	_NAmpHDOut	-450.947	-225.433	0	0
25	_HnD2	_NAmpHD2-	-450.947	-225.433	0	0
26	_HnD1	_NAmpHD1+	-450.948	-225.433	-1	0
31	HnS1	NAmpHS1+	-450.939	-225.433	8	0
32	HnS2	NAmpHS2-	-450.947	-225.433	0	0
33	HnS3	NAmpHSOut	-450.947	-225.433	0	0
34	_HnS3	_NAmpHSOut	-450.947	-225.433	0	0
35	_HnS2	_NAmpHS2-	-450.947	-225.434	0	-1
36	_HnS1	_NAmpHS1+	-450.956	-225.434	-9	-1

Simulation #	Sch Name	Amp A Capacitors: Odd Stage	Hold [mV] @19us 2x Out	DAC [mV] @ 18us DAC Out	Error [µV] @19us 2x Out	Error [µV] @ 18us DAC Out	
0		**BaseLine**	**-450.947**	**-225.433**			
1	ApRo	CPRoA	-450.947	-225.433	0	0	
2	_ApRo	_CPRoA	-450.947	-225.433	0	0	
3	AnRo	CNRoA	-450.947	-225.433	0	0	
4	_AnRo	_CNRoA	-450.947	-225.434	0	-1	
5	AC+	CapA+	-450.757	-225.339	190	94	** Both → 0
6	_AC+	_CapA+	-450.751	-225.336	196	97	** Both → 0
7	AC-	CapA-	-450.757	-225.338	190	95	** Both → 0
8	_AC-	_CapA-	-450.756	-225.338	191	95	** Both → 0
9	Acm	CAmpAos	-450.948	-225.434	-1	-1	
10	_Acm	_CAmpAos	-450.947	-225.434	0	-1	

Note: Sampling Capacitors AC+ & AC- are before double sampling error removal

** Error is eliminated with double sampling

Simulation #	Sch Name	Amp B Capacitors: Even Stage	Hold [mV] @19us **2x Out**	DAC [mV] @ 18us **DAC Out**	Error [µV] @19us **2x Out**	Error [µV] @ 18us **DAC Out**	
0		**BaseLine**	**-450.947**	**-225.433**			
1	BpRo	CPRoB	-450.947	-225.433	0	0	
2	_BpRo	_CPRoB	-450.947	-225.433	0	0	
3	BnRo	CNRoB	-450.947	-225.433	0	0	
4	_BnRo	_CNRoB	-450.947	-225.433	0	0	
5	BC+	CapB+	-450.686	-225.303	261	130	** Both → 0
6	_BC+	_CapB+	-450.677	-225.298	270	135	** Both → 0
7	BC-	CapB-	-450.684	-225.302	263	131	** Both → 0
8	_BC-	_CapB-	-450.682	-225.301	265	132	** Both → 0
9	Bcm	CAmpBos	-450.948	-225.434	-1	-1	
10	_Bcm	_CAmpBos	-450.946	-225.433	1	0	

Note: Sampling Capacitors BC+ & BC- are before double sampling error removal

** Error is eliminated with double sampling

Simulation #	Sch Name	Amp H Capacitors: Output Amplifier	Hold [mV] @19us 2x Out	DAC [mV] @ 18us DAC Out	Error [µV] @19us 2x Out	Error [µV] @ 18us DAC Out
0		**BaseLine**	**-450.951**	**-225.433**		
1	**HpRo**	CPRoA2	-450.951	-225.433	0	0
2	**_HpRo**	_CPRoA2	-450.951	-225.433	0	0
3	**HnRo**	CNRoA2	-450.951	-225.433	0	0
4	**_HnRo**	_CNRoA2	-450.951	-225.433	0	0
5	**HC**	CapA2	-450.948	-225.433	3	0
6	**_HC**	_CapA2	-450.945	-225.433	6	0
7	**Hcm**	CAmpA2os	-450.951	-225.433	0	0
8	**_Hcm**	_CAmpA2os	-450.951	-225.433	0	0
9	**Hhold**	CapOutA2	-450.951	-225.433	0	0
10	**_Hhold**	_CapOutA3	-450.951	-225.433	0	0

Note: This is the more rugged core ADC 1-bit stage (2x residue gain stage)

Simulation #	Sch Name	A Switches: Odd Stage	Hold [mV] @19us 2x Out	DAC [mV] @ 18us DAC Out	Error [µV] @19us 2x Out	Error [µV] @ 18us DAC Out
0		**BaseLine**	**-450.947**	**-225.433**		
1	Asmp+P	PInA++	-450.946	-225.433	1	0
2	Aout1P	POutA++	-450.947	-225.434	0	-1
3	_Aout1P	_POutA++	-450.947	-225.433	0	0
4	_Asmp+P	_PInA++	-450.949	-225.434	-2	-1
11	Asmp+N	NInA++	-450.948	-225.433	-1	0
12	Aout1N	NOutA++	-450.947	-225.433	0	0
13	_Aout1N	_NOutA++	-450.947	-225.433	0	0
14	_Asmp+N	_NInA++	-450.946	-225.433	1	0
21	Init+P	PInit+-	-450.947	-225.434	0	-1
22	AsmpP	PInA+-	-450.948	-225.434	-1	-1
23	Afb1P	POutA+-	-450.944	-225.432	3	1
24	_Afb1P	_POutA+-	-450.951	-225.436	-4	-3
25	_AsmpP	_PInA+-	-450.946	-225.433	1	0
26	_Init+P	_PInit+-	-450.948	-225.434	-1	-1
31	Init+N	NInit+-	-450.947	-225.433	0	0
32	AsmpN	NInA+-	-450.945	-225.433	2	0
33	Afb1N	NOutA+-	-450.952	-225.436	-5	-3
34	_Afb1N	_NOutA+-	-450.943	-225.432	4	1
35	_AsmpN	_NInA+-	-450.950	-225.435	-3	-2
36	_Init+N	_NInit+-	-450.947	-225.433	0	0
41	Init-P	PInit-+	-450.947	-225.433	0	0
42	Aout2P	POutA-+	-450.947	-225.433	0	0
43	_Aout2P	_POutA-+	-450.947	-225.433	0	0
44	_Init-P	_PInit-+	-450.947	-225.433	0	0

Simulation #	Sch Name	A Switches: Odd Stage	Hold [mV] @19us 2x Out	DAC [mV] @ 18us DAC Out	Error [µV] @19us 2x Out	Error [µV] @ 18us DAC Out
0		**BaseLine**	**-450.947**	**-225.433**		
51	Init-N	NInit-+	-450.947	-225.433	0	0
52	Aout2N	NOutA-+	-450.947	-225.433	0	0
53	_Aout2N	_NOutA-+	-450.947	-225.433	0	0
54	_Init-N	_NInit-+	-450.947	-225.434	0	-1
61	Asmp-P	PInA--	-450.949	-225.434	-2	-1
62	Afb2P	POutA--	-450.943	-225.432	4	1
63	_Afb2P	_POutA--	-450.951	-225.435	-4	-2
64	_Asmp-P	_PInA--	-450.945	-225.433	2	0
71	Asmp-N	NnA--	-450.944	-225.433	3	0
72	Afb2N	NOutA--	-450.952	-225.436	-5	-3
73	_Afb2N	_NOutA--	-450.943	-225.432	4	1
74	_Asmp-N	_NnA--	-450.950	-225.435	-3	-2
81	ArefP	PAmp5ASu	-450.947	-225.433	0	0
82	AcmP	PAmp0ASu	-450.949	-225.434	-2	-1
83	AsuP	PAmpASs	-450.968	-225.444	-21	-11
84	_AsuP	_PAmpASs	-450.926	-225.423	21	10
85	_AcmP	_PAmp0ASu	-450.947	-225.433	0	0
86	_ArefP	_PAmp5ASu	-450.945	-225.433	2	0
91	ArefN	NAmp5ASu	-450.947	-225.433	0	0
92	AcmN	NAmp0ASu	-450.945	-225.433	2	0
93	AsuN	NAmABSs	-450.926	-225.423	21	10
94	_AsuN	_NAmpASs	-450.968	-225.444	-21	-11
95	_AcmN	_NAmp0ASu	-450.947	-225.433	0	0
96	_ArefN	_NAmp5ASu	-450.949	-225.434	-2	-1

Simulation #	Sch Name	B Switches: Even Stage	Hold [mV] @19us 2x Out	DAC [mV] @ 18us DAC Out	Error [µV] @19us 2x Out	Error [µV] @ 18us DAC Out
0		**BaseLine**	**-450.947**	**-225.433**		
1	Bsmp+P	PInB++	-450.946	-225.433	1	0
2	Bout1P	POutB++	-450.946	-225.433	1	0
3	_Bout1P	_POutB++	-450.949	-225.433	-2	0
4	_Bsmp+P	_PInB++	-450.948	-225.434	-1	-1
11	Bsmp+N	NInB++	-450.948	-225.434	-1	-1
12	Bout1N	NOutB++	-450.948	-225.433	-1	0
13	_Bout1N	_NOutB++	-450.946	-225.433	1	0
14	_Bsmp+N	_NInB++	-450.947	-225.433	0	0
21	BsmpP	PInB+-	-450.949	-225.435	-2	-2
22	Bfb1P	POutB+-	-450.940	-225.430	7	3
23	_Bfb1P	_POutB+-	-450.954	-225.437	-7	-4
24	_BsmpP	_PInB+-	-450.944	-225.432	3	1
31	BsmpN	NInB+-	-450.943	-225.431	4	2
32	Bfb1N	NOutB+-	-450.955	-225.438	-8	-5
33	_Bfb1N	_NOutB+-	-450.940	-225.429	7	4
34	_BsmpN	_NInB+-	-450.952	-225.436	-5	-3
41	Bout2P	POutB-+	-450.946	-225.433	1	0
42	_Bout2P	_POutB-+	-450.949	-225.433	-2	0
1	Bsmp+P	PInB++	-450.946	-225.433	1	0

Simulation #	Sch Name	B Switches: Even Stage	Hold [mV] @19us 2x Out	DAC [mV] @ 18us DAC Out	Error [µV] @19us 2x Out	Error [µV] @ 18us DAC Out
0		**BaseLine**	**-450.947**	**-225.433**		
51	Bout2N	NOutB-+	-450.948	-225.433	-1	0
52	_Bout2N	_NOutB-+	-450.947	-225.434	0	-1
61	Bsmp-P	PInB--	-450.950	-225.435	-3	-2
62	Bfb2P	POutB--	-450.940	-225.430	7	3
63	_Bfb2P	_POutB--	-450.955	-225.437	-8	-4
64	_Bsmp-P	_PInB--	-450.944	-225.432	3	1
71	Bsmp-N	NnB--	-450.941	-225.431	6	2
72	Bfb2N	NOutB--	-450.955	-225.438	-8	-5
73	_Bfb2N	_NOutB--	-450.940	-225.429	7	4
74	_Bsmp-N	_NnB--	-450.953	-225.437	-6	-4
81	BrefP	PAmp5BSu	-450.947	-225.434	0	-1
82	BcmP	PAmp0BSu	-450.950	-225.435	3	2
83	BsuP	PAmpBSs	-450.988	-225.454	-41	-21
84	_BsuP	_PAmpBSs	-450.906	-225.413	41	20
85	_BcmP	_PAmp0BSu	-450.947	-225.433	0	0
86	_BrefP	_PAmp5BSu	-450.944	-225.432	3	1
91	BrefN	NAmp5BSu	-450.947	-225.433	0	0
92	BcmN	NAmp0BSu	-450.943	-225.431	4	2
93	BsuN	NAmpBSs	-450.904	-225.412	43	21
94	_BsuN	_NAmpBSs	-450.990	-225.455	-43	-22
95	_BcmN	_NAmp0BSu	-450.947	-225.433	0	0
96	_BrefN	_NAmp5BSu	-450.951	-225.435	-4	-2
51	Bout2N	NOutB-+	-450.948	-225.433	-1	0

Simulation #	Sch Name	H Switches:	Hold [mV] @19us 2x Out	DAC [mV] @ 18us DAC Out	Error [µV] @19us 2x Out	Error [µV] @ 18us DAC Out
0		**BaseLine**	**-450.947**	**-225.433**		
1	Hin+P	PInH+	-450.946	-225.433	1	0
11	Hin+N	NInH+	-450.946	-225.433	1	0
21	Hin-P	PInH-	-450.950	-225.434	-3	-1
31	Hin-N	NInH-	-450.944	-225.434	3	-1
41	HcmP	PAmp0HSu	-450.950	-225.433	-3	0
51	HcmN	NAmp0HSu	-450.944	-225.433	3	0
61	HholdP	POutA	-450.947	-225.433	0	0
71	HholdN	NOutA	-450.947	-225.433	0	0
2	HoutP	POutH+	-450.947	-225.433	0	0
12	HoutN	NOutH+	-450.947	-225.433	0	0
22	HfbP	POutH-	-450.942	-225.433	5	0
32	HfbN	NOutH-	-450.954	-225.433	-7	0
42	HsuP	PAmpHSs	-450.963	-225.433	-16	0
52	HsuN	NAmpHSs	-450.931	-225.433	16	0
62	_HholdP	_POutA	-450.947	-225.433	0	0
72	_HholdN	_NOutA	-450.947	-225.433	0	0
4	_Hin+P	_PInH+	-450.948	-225.434	-1	-1
14	_Hin+N	_NInH+	-450.947	-225.433	0	0
24	_Hin-P	_PInH-	-450.945	-225.433	2	0
34	_Hin-N	_NInH-	-450.951	-225.433	-4	0
44	_HcmP	PAmp0HSu	-450.944	-225.433	3	0
54	_HcmN	_NAmp0HSu	-450.950	-225.433	-3	0
3	_HoutP	_POutH+	-450.947	-225.433	0	0
13	_HoutN	_NOutH+	-450.947	-225.433	0	0
23	_HfbP	_POutH-	-450.953	-225.434	-6	-1
33	_HfbN	_NOutH-	-450.941	-225.433	6	0
43	_HsuP	_PAmpHSs	-450.930	-225.433	17	0
53	_HsuN	_NAmpHSs	-450.964	-225.433	-17	0

Temperature	2x Output Hold [mV]	DAC Output DAC [mV]	2x Out Error [µV]	DAC Out Error [µV]
°C	@19us	@ 18us	@19us	@ 18us
Baseline	**-450.947**	**-225.433**		
-125	-450.933	-225.434	14	-1
-100	-450.941	-225.433	6	0
-75	-450.945	-225.433	2	0
-50	-450.947	-225.433	0	0
-25	-450.947	-225.433	0	0
0	-450.947	-225.433	0	0
25	-450.947	-225.433	0	0
50	-450.947	-225.433	0	0
75	-450.947	-225.433	0	0
100	-450.947	-225.433	0	0
125	-450.947	-225.433	0	0
150	-450.955	-225.435	-8	-2
175	-450.991	-225.446	-44	-13
200	-451.027	-225.499	-80	-66
225	-452.112	-225.926	-1165	-493
250	-448.191	-223.469	2756	1964

Process Parameter			**2x Output Hold [mV]**	**DAC Output DAC [mV]**	**2x Out Error [µV]**	**DAC Out Error [µV]**
Case	NMOS	PMOS	@ 38µs	@ 35.5µs	@ 38µs	@ 35.5µs
1	**Typ**	**Typ**	**-450.949**	**-225.434**	**0**	**0**
2	Fast	Fast	-450.944	-225.431	5	3
3	Slow	Slow	-450.949	-225.434	0	0
4	Fast	Slow	-450.957	-225.437	-8	-3
5	Slow	Fast	-450.941	-225.431	8	3

Vdd	2x Output Hold [mV]	DAC Output DAC [mV]	Ck Period	2x Out Error [µV]	DAC Out Error [µV]	Fast Conversion Capability	Supply Current	Power Consumption
Volts	@19us	@ 18us		@19us	@ 18us		µa	µW
Baseline	**-225.981**	**-112.886**						
2.0	-225.981	-112.886	1us	0	0	10,000,000	1,195.600	700.000
1.9	-225.981	-112.886	1us	0	0	10,000,000	936.987	560.000
1.8	-225.981	-112.886	1us	0	0	10,000,000	740.650	450.000
1.7	-225.981	-112.886	1us	0	0	9,500,000	555.341	350.000
1.6	-225.980	-112.885	1us	1	1	8,500,000	404.664	270.000
1.5	-225.977	-112.882	1us	4	4	7,000,000	283.789	190.000
1.4	-225.972	-112.877	1us	9	9	5,000,000	186.728	133.377
1.3	-225.966	-112.872	1us	15	14	3,200,000	113.301	85.000
1.2	-225.960	-112.867	1us	21	19	1,900,000	62.354	49.000
1.1	-225.953	-112.861	10us	28	25	1,000,000	27.508	24.000
1.0	-225.953	-112.861	10us	28	25	480,000	10.126	9.500
0.9	-225.970	-112.875	10us	11	11	200,000	2.917	3.200
0.8	-225.992	-112.897	100us	-11	-11	65,000	0.655	0.818
0.7	-226.008	-112.913	1ms	-27	-27	16,000	0.138	0.205
0.6	-226.018	-112.925	1ms	-37	-39	3,200	0.029	0.049
0.5	-226.027	-112.936	2ms	-46	-50	500	0.006	0.012

Note: Errors are generally a settling time issue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